TECHNICAL MANUAL model ACT-V

MICRO-TERM, INC.

ST. LOUIS, MISSOURI 63144

ACT-V

TECHNICAL MANUAL

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1. GENERAL DESCRIPTION OF THE ACT-V

The ACT-V computer terminal provides a communication channel between humans and computers. It is equipped with many features that facilitate the man-machine interface. Figure 1.1 presents the ACT-V block diagram. There are seven major circuits in the ACT-V. These are:

1) Power Supply
2) Keyboard
3) Input/Output Interfaces
4) Microprocessor Control Unit
5) Synchronization Generator
6) Refresh Display Memory
7) Video Generator

Each of these circuits is described in detail in the later sections of this manual. In this section the operation of the ACT-V will be discussed at the block-diagram level. Circuit diagrams and other technical data can be found in the Appendices.

First, each of the seven circuits will be briefly described. Then the interactions between the circuits will be demonstrated through descriptions of the two basic terminal functions; i.e. receiving/displaying characters and keying/sending characters.

1.1 Power Supply

The ACT-V power supply produces +5 volts at 1.5 amps, +12 volts at 200ma and -12 volts at 250ma. Minus five volts is derived from minus twelve in the video generator circuit.

1.2 Keyboard

The ACT-V keyboard uses a scanning encoding technique to generate the ASCII character set. Several keys on the keyboard are auto-repeating. When they are held down for more than one second the keyboard circuit generates a series of strobe pulses at the rate of 15 characters per second.

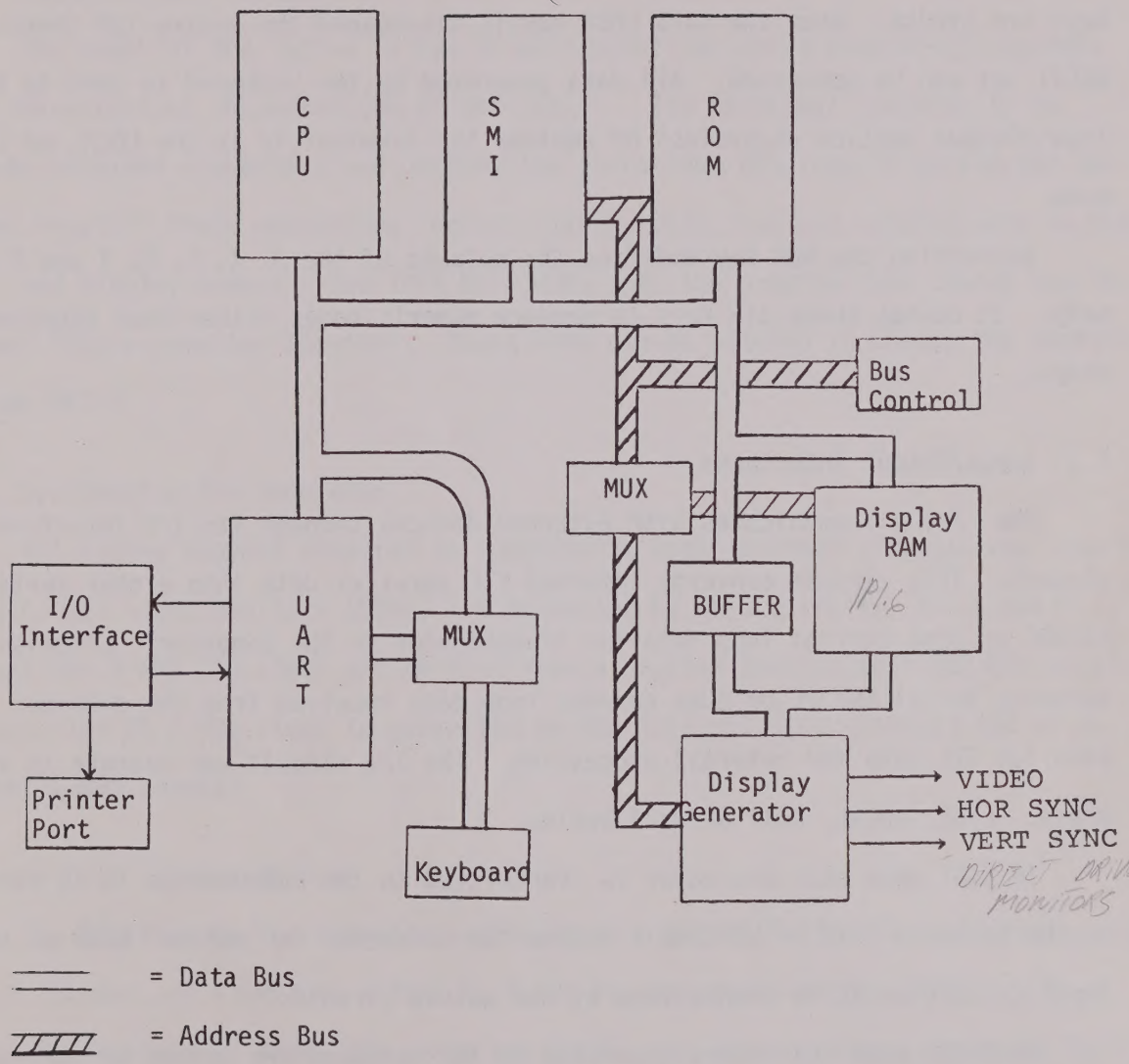


Figure 1.1: ACT-V Block Diagram

Auto repeat keys are Space, ⇄, ↑↓ and period. Any key may be made to repeat by first depressing it and then holding the repeat key down. The CAPS LOCK key forces the keyboard to generate only upper case alphabetic codes when alphabetic keys are struck. When the CAPS LOCK key is disengaged the entire 128 character ASCII set can be generated. All data generated by the keyboard is sent to the Input/Output section regardless of whether the terminal is in the LOCAL or LINE mode.

Depressing the NUM key modifies the outputs of the J, K, L, U, I and O keys only. It causes these six keys to produce numeric codes rather than alphabetic codes.

1.3 Input/Output Interfaces

The ACT-V communicates with external devices through its I/O interface circuit. This circuit converts internal TTL parallel data into either serial RS232C or 20ma current loop data for transmission to the computer. Likewise it converts serial RS232C or 20ma current loop data received from the computer into parallel TTL data for internal processing. The I/O circuit can operate in several modes: LINE, LOCAL, Full or Half Duplex.

In LINE mode each character is transmitted to the computer as it is struck on the keyboard. If in LINE/Half Duplex the character is "echoed" back to the Input circuit as it is transmitted by the output circuit.

In LOCAL mode characters generated by the keyboard are echoed to the receiver circuit but are not transmitted to the computer until either the SEND key or the SHIFT SEND keys are depressed. This permits use of the ACT-V editing features. While in the LOCAL mode characters sent by the computer are displayed on the ACT-V screen.

A Printer Port output facilitates local hard copy output by providing a serial RS232C output port to a printer.

Data rates and UART options are conveniently switch selectable to modify various communications parameters.

1.4 Microprocessor Control Unit

The heart of the ACT-V is the F8 microprocessor which completely controls and characterizes the operation of the ACT-V. Its principal function is to decode received characters and perform the operations required to obtain the desired result. These operations include reading data from and writing data to the UART and display memory. Two 1024 by 8 ROMs hold the program that causes the F8 to act like a computer terminal. These ROMs can be altered to change the operation of the ACT-V.

1.5 Synchronization Generator

All timing signals required to synchronize both internal circuits and internal or external video monitors (CRTs) are generated by this circuit. All signals except the 2 MHz CPU clock are derived from a crystal controlled 9.828 MHz oscillator. The F8 2 MHz clock is generated by its internal clock circuit and an external 2 MHz crystal.

1.6 Refresh Display Memory

The ASCII codes for characters displayed in the 1920 (80x24) positions on the ACT-V screen are stored in a 2048 by 9 bit random access memory (RAM). Nine bits are required to store the seven bit ASCII code plus a cursor bit and a full/half intensity (Un/Protected) bit. This refresh RAM is shared by the F8 and the video generator circuit. The F8 both reads and writes from and to the RAM while the video generator only reads from the RAM.

1.7 Video Generator

The video generator circuit reads ASCII data from the refresh RAM and generates a dot pattern for display on the monitor. This circuit generates a video signal for

direct drive (or data display) monitors.

Further details concerning the operation of the above circuits can be found in the following sections of this manual.

1.8 Operating Examples

The operating examples discussed in this section indicate the manner in which the various blocks in the ACT-V block diagram of Figure 1.1 interact to perform the required operation.

1.8.1 Receiving/Displaying Characters

When the UART assembles a complete ASCII character it raises its data available flag and interrupts the F8. The F8 reads the character from the UART into its accumulator and resets the UART flag.

The character is then tested to determine if it is a displayable or a control character. If it is displayable the F8 waits until the next horizontal retrace period, takes control of the multiplexed address lines to the display RAM and writes the character into the RAM with the cursor bit low. During the next horizontal sync pulse the F8 takes control of the RAM address lines and reads the character code stored in the position where the cursor is to be moved. The cursor bit is set and the character is replaced during still another horizontal retrace pulse. The maximum time required to perform these operations is 192usec (64x3).

If the received character causes a scroll operation (i.e. it is either the 80th character to be loaded on the bottom line or a line feed code) the execution time is increased to approximately 700 usec. After loading the character in the display memory the F8 waits to be interrupted by the UART flag when the next character is received.

When the ACT-V receives control characters from either its keyboard (in the Local mode) or from the external computer it responds as programmed in the 2708

Master Control ROMs (MPB,PT).

1.8.2 Keying/Sending Characters

When in the on LINE mode of operation the ACT-V keyboard has control of the transmitter half of the I/O UART at all times except for a few moments when the F8 takes control to report the cursor position after receiving such a request. Each character is transmitted as soon as the key is struck. If the half duplex mode has been selected the characters will be presented simultaneously to the external computer and the ACT-V I/O UART for immediate display (local echo).

In the Local mode characters typed on the ACT-V keyboard are locally echoed but are not sent to the external computer until the SEND key or the SHIFT SEND keys are depressed. When the F8 receives this locally echoes send command it commences passing the required amount of data to the UART for transmission to the external computer. During this time characters typed on the keyboard are not transmitted or echoed locally.

2. POWER SUPPLY

The ACT-V power supply generates the following D.C. voltages: +12v, +5v, -5v, and -12v. The power supply is fed by a transformer with dual primaries (to allow for either 110 or 220 volt operation) and dual center-tapped secondaries. The secondaries are both rated at 12.6 volts, 2.5 amps. The first secondary (Red, Red/Yel, Red) provides AC power to the -12 and -5volt supplies for the main board and also provides current to the +12 volt monitor and main board supplies. The other secondary provides AC power to the +5 volt supply for the logic on the main board.

2.1 Minus Voltage Supplies

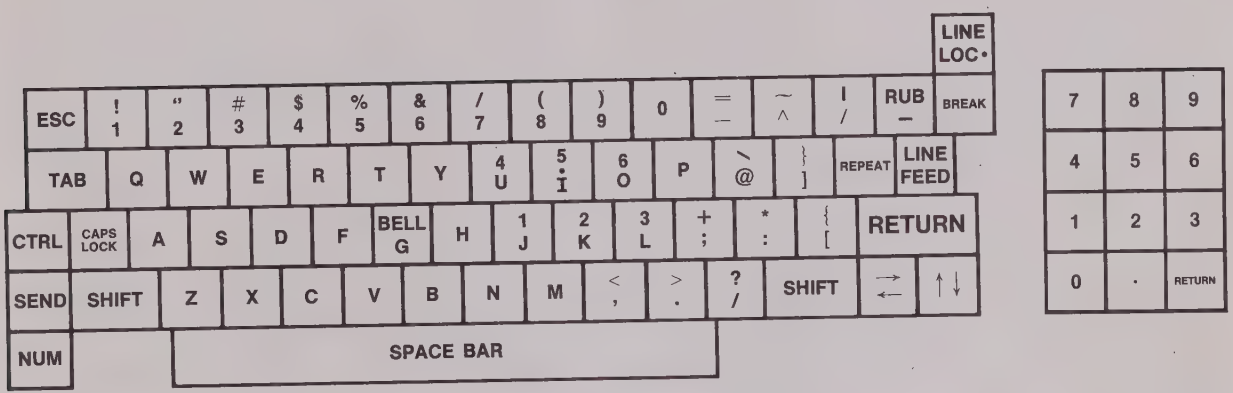
Both the -12 and -5 volt supplies are lightly loaded and consequently are implemented with zener diodes and pass transistors. They are not short circuit protected.

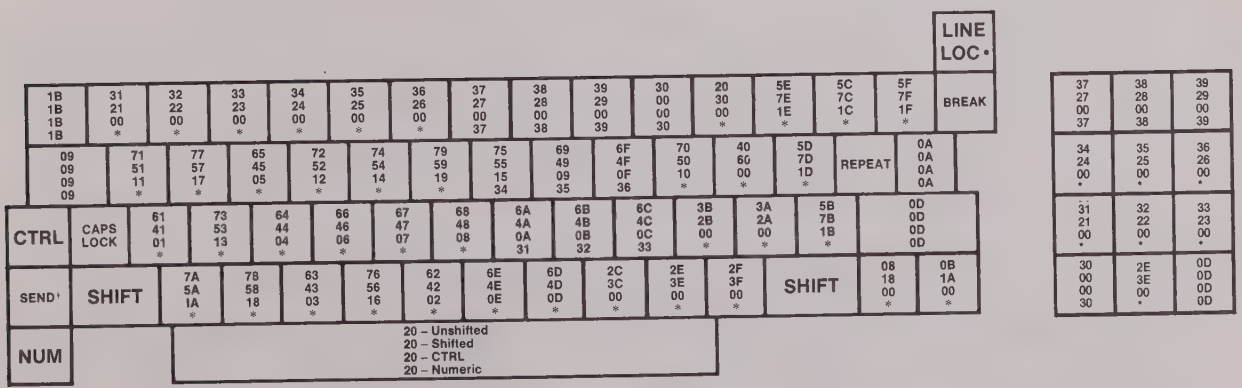
2.2 Plus Voltage Supplies

The +12 and +5 volt power supplies are also of the pass transistor type; however, each of these employs an operational amplifier to provide feedback for regulation rather than rely on zener diode regulation. The positive supplies are not short circuit protected; however, high power zener diodes (D8 and D9) are placed across their outputs to protect the logic circuits from overvoltage conditions. The pass transistors Q10 and Q11 are mounted to the ACT-V chassis (with insulating hardware) allowing the cabinet to act as a heat sink.

3. KEYBOARD

The ACT-V keyboard is capable of generating the complete set of ASCII codes (0-7F Hex). The assignment of ASCII codes to keyswitches is listed below. Keyswitches are either auto repeating or regular.





3.1 Encoding Regular Keys

The ACT-V uses a grid scanning routine to encode the keyboard. CNT2 provides address information to D.S.1 and D.S.2. When a key is depressed one of the output lines from D.S.1 will be shorted to one of the input pins of D.S.2 and D.S.2 pin 3 will go high for the duration the key is held down. This rising signal is delayed by C5 and applied to the base of Q2 which drives the A input of O.S.1. O.S.1 is a retriggerable one-shot with a period of 8ms (determined by R14 and C3). This period is long enough to prevent keybounce from generating multiple strobes. When O.S.1a fires and its $\overline{Q}$ output drops low CNT2 is halted with a count value that corresponds to the depressed key. This value provides six of the ten address lines to a 1k by 8 ROM (MKE). The other four address lines are provided by the CAPS LOCK, NUM, CTRL and SHIFT keyswitches. MKE performs a table look-up to produce the required ASCII code at its parallel outputs (D0 through D6). The output at D7 indicates whether the key is auto-repeating or not (see Section 3.2 below). When O.S.1a fires it triggers O.S.1b which generates a 300usec strobe pulse.

3.2 Repeat Function

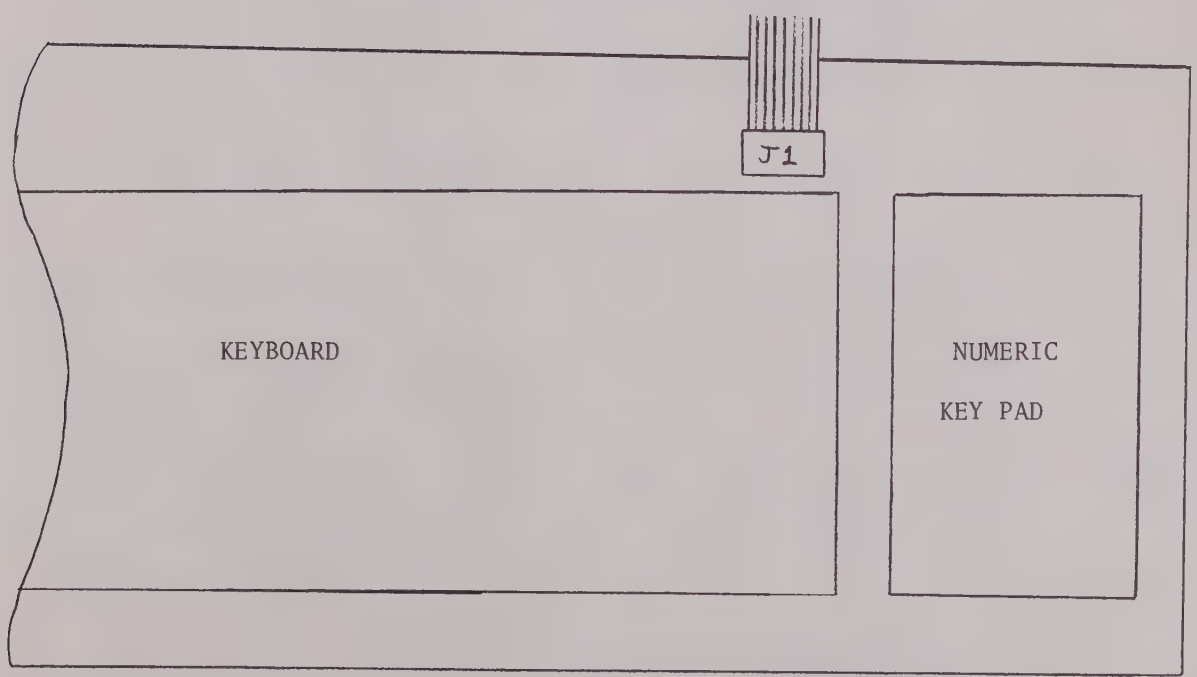
O.S.1b can be forced to generate multiple strobe pulses by sending a pulse train into its A trigger input from the selected output of CNT 1. The standard repetition rate of 15 characters per second is implemented by dividing the 60Hz display enable signal by four at CNT1p11. CNT1 is normally held to the zero state by virtue of pin 2 (reset) being pullsed up to +5 through R5 and D2. When an auto-repeating key is held down MKEp17 (D7) goes low and discharges C1 through R8. After about one second the voltage at CNT1p2 is sufficiently low to enable the counter and produce multiple strobes. Regular keys may be made to repeat by depressing the REPEAT key. This also discharges C1 and enables CNT1.

3.3 Cursor Control Keys

Since the ASCII code - keyswitch assignment of the ACT-V keyboard is set by MKE it is not possible to have the cursor control keys to generate codes required by all of the four terminals that the ACT-V is capable of mimicing. The output codes for the ⇆ and ↑↓ keys are those specified by the ACT- V cursor control feature. The keyboard code assignments may be altered by modifying the contents of the MKE (ACT-V Keyboard Encoder) ROM.

3.4 Insertion of Cable Into J1

The proper orientation of the ribbon connector in socket J1 is illustrated below:



4. INPUT/OUTPUT CIRCUITS

The input/output (I/O) circuits of the ACT-V establish all necessary communications links between the terminal and remote devices such as computers or modems. The serial to parallel and parallel to serial conversions that are required to permit communication between the parallel-bus oriented ACT-V and serial ASCII oriented computer interfaces are performed in the I/O circuits.

4.1 I/O UART

All serial communications to and from the I/O and printer ports on the ACT-V are processed by the I/O UART (U1). Relevant UART pin assignments and functions are listed below.

Pin Number	Name (Symbol)	Function
4	$\overline{\text{Received Data Enable(RDE)}}$	A logic 0 places the received data onto the F-8 data bus.
5-12	Received Data Bits(RD8-RD1)	Tri-state data out lines. LSB of ASCII code appears at RD1 (pin 12).
17	Receiver clock	Clock of 16 times the desired data rate.
18	$\overline{\text{Reset Data Available(RDAV)}}$	A low pulse on this line will reset the data available flag (pin 19).
19	Data Available(DAV)	This line goes to a logical 1 when an entire character has been received and transferred to the tri-tate receiver holding register.
20	Serial Data Input(SI)	This line accepts the serial input data. A marking (logical 1) to spacing (logical 0) transition is required for initiation of data reception.
22	Transmitter Buffer empty(TBE)	This tri-state line goes high when the transmitter is ready to accept another character.
23	$\overline{\text{Data Strobe(DS)}}$	A strobe on this line loads a character into the transmitter buffer. Transmission is initiated by the rising edge of $\overline{\text{DS}}$.

Pin Number	Name (Symbol)	Function
24	End of Character(EOC)	This line goes to a logic 1 each time a full character is transmitted. It remains there until the start of transmission of the next character.
25	Serial Output(SO)	This line will serially provide the entire transmitted character. When not transmitting this line stays at a logical 1.
26-33	Data Bit Inputs(DB1-DB8)	There are up to 8 data bit input lines available.
35	No parity(NP)	A logic 1 on this line inhibits transmission of the parity bit.
36	Number of Stop Bits	A logic 1 selects 2 stop bits, a logic 0 selects 1 stop bit.
37,38	Number of Bits/Char(NB2,NB1)	These leads determine the number of data bits to be transmitted per character, as follows: NB2 NB1 # of Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select(EPS)	A logic 1 selects even parity, a logic 0 selects odd parity.
40	Transmitter Clock(TCP)	This line is driven by a clock rate of 16 times the desired data rate.

Proper selection of the UART option switches attached to pins 35-39 can be achieved by referring to Section 4.7 of the ACT-V Operation Manual.

4.2 Character Transmission from the Keyboard in LINE Mode

When the ACT-V is operating in the LINE mode characters are transmitted when the keys are struck. Either half or full duplex transmission can be selected.

4.2.1 Half Duplex Operation

In half duplex the keyboard strobe (J1p8, STR) sets FF3 and forces the data

strobe input of the UART (U1p23) low through data switch D.S.4p12 since the keyboard has been selected to provide the inputs to the transmitter section of the UART. This selection is made by the F8. The keyboard is normally chosen unless the F8 needs to send characters out in the block transmit mode. The keyboard strobe pulse sets FF3 to indicate the character originated from the keyboard. When U1p23 ($\overline{DS}$) returns high the character data present at U1p26-32 is transmitted serially out U1p25. The serial data out at U1p25 is normally marking (logical 1 = +5v). It drives two inputs on DS6 (pins 2 and 13). Depending on whether the CPU has selected the I/O or the printer as the destination port (via CPUp31 to D.S.6p1) the serial data will emerge at either DS6p12 or DS6p4. Printer port serial data at DS6p4 drives a TTL to RS232C level converter consisting of R18, 19, 20 and Q7. The RS232C output of this circuit drives an external printer via pin 14 of the 25 pin EIA connector (I/O Conn p 14). The operation of the printer port is described further in Section 4.7 below. Serial data emerging at DS6p12 provides one of the five inputs to CR2 (control ROM). Table 4.1 lists the other inputs and outputs of CR2. Figure 4.1 illustrates the operation of CR2. In the on line, half duplex mode serial data at CR2p14 is passed on to both CR2p4 (for transmission out of the ACT-V via OA2p8 and I/O Conn p 2 for RS232C or via ISO2, FWB2 and I/O Conn p 10, 11 for loop out and CR2p1 for internal echo. Note that if the current loop interface has been enabled and no current is flowing in the loop in of the ACT-V CR2p12 will be low and will prevent the internal echo of data in either the half duplex or local modes due to the manner in which these signals are gated internally in CR2.

INPUTS TO CR2	PIN #
I/O Serial Data Out (H=Mark)	14
I/O Serial Data In (L=Mark)	13
Current Loop In (L=Mark)	12
Line/$\overline{\text{Local}}$ (H=Line)	11
Full/Half Duplex (H=Full)	10
OUTPUTS OF CR2	
Serial Data In (To UART)	1
Current Loop Out (L=Mark)	2
$\overline{\text{Line}}$/Local (L=Line)	3
Serial Data Out (L=Mark)	4

Table 4.1: Inputs and Outputs of CR2

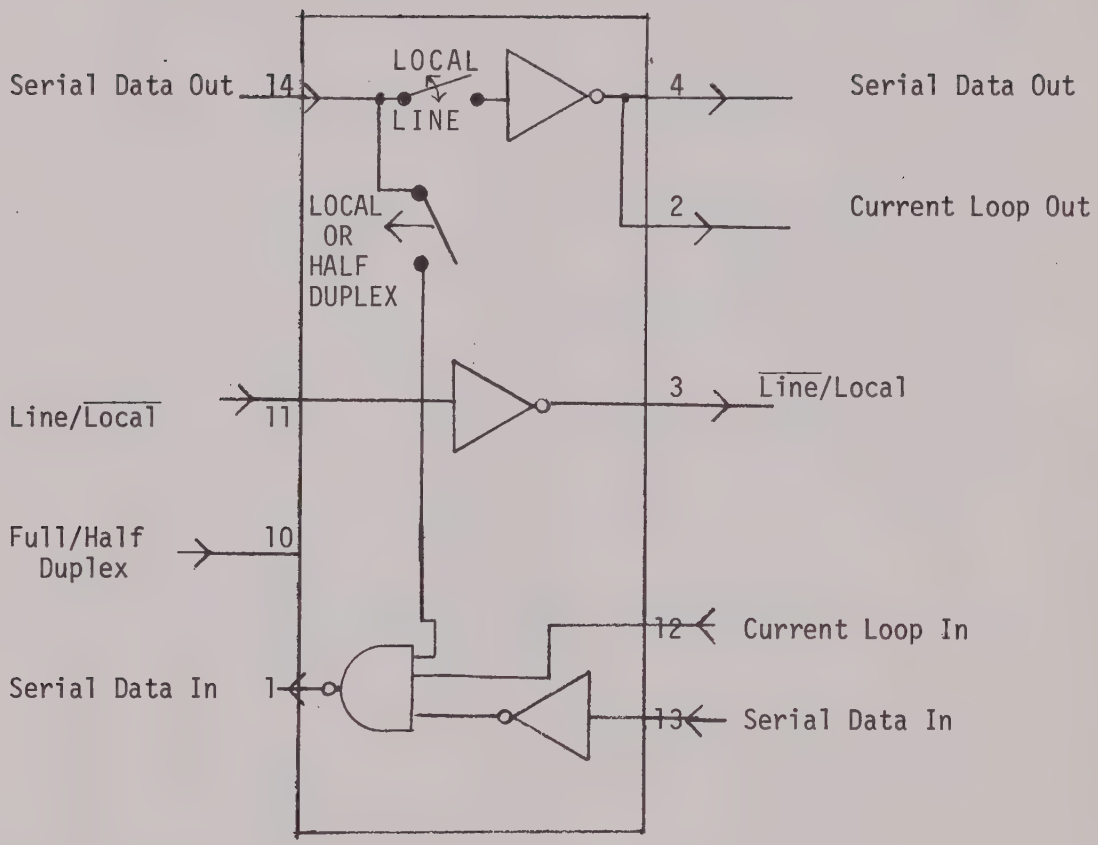


Figure 4.1: CR2 Functional Diagram

4.2.2 Full Duplex Operation

In the full duplex mode serial data at CR2p14 is routed only to CR2 pins 2 and 4. There is no internal echo unless the LINE/LOC· switch is in the LOC(al) position.

4.3 RS232C Interface

Two of the four operational amplifiers in OA2 are used to provide an RS232C line driver and receiver. Serial data at U1p25 is routed to CR2p4 as described in the previous paragraphs. When U1p25 is in the mark (logical 1) state CR2p4 and OA2p9 are low (zero volts). OA2p10, 6, 2 and 13 are all held at approximately 1.5 volts by the voltage divider circuit of R15 and R16. This voltage provides a threshold reference for all four amplifiers in OA2. The combination of a low level at OA2p9 and a higher level at OA2p10 forces OA2p8 to -12 volts (an RS232C mark). When U1p25 is in the space state OA2p8 is high (+5 volts). The BREAK key holds the serial output in the space state when it is depressed.

RS232C serial data into the ACT-V at I/O Conn p 3 is fed to OA2p5 where it is compared to the 1.5 volt reference. When no connection is made to I/O Conn p 3 R28 holds that line in mark state.

4.4 Block Mode Transmission in LOCAL Mode

When operating in the LOCAL mode CR2 echoes data back to the receiver half of the UART for immediate display and no data is sent out the ACT-V serial out lines (RS232C or Current Loop) until the SEND key is depressed either alone or in conjunction with the SHIFT key. Depressing the SEND key forces the ACT-V into the LOCAL mode and also sends the code 1C hex to the UART receiver.

The F8 recognized this and sends all of the full intensity characters on the line containing the cursor. This is accomplished by pulling the select line of DS4 and DS5 and CR2p11 high. This allows the F8 data bus to drive the UART transmitter buffer inputs and also forces the I/O circuit into the line mode regardless

of the position of the LINE/LOC· switch.

Before sending each character in the block mode the F8 samples the Data Set Ready (DSR) line at pin 6 of the I/O Connector and will not transmit until this line assumes the high state. If the external device (modem or computer) does not use this line to indicate readiness R25 will hold the line high to permit transmission. If for some reason I/O Conn p 6 is grounded and a SEND or SHIFT SEND operation is initiated the ACT-V will enter an "infinite loop" waiting for this line to rise. When transmission is completed the ACT-V sounds its beeper.

4.5 UART Clock Generation

The clock rates of 16 times (16x) the desired serial bit (baud) rate are generated by a digital divide-down chain which is driven by the dot-oscillator of the ACT-V. This dot oscillator's frequency is 9.828 MHz.

A 7493 divide-by-eight counter, CNT7, provides a 1.2 MHz square wave into CNT9. CNT9 is a binary counter that divides the 1.2 MHz signal from CNT7 by successive factors of two and yields the 16x clock rates for 9600 B/S to 300 B/S at the following pins:

Data Rate (Bits/sec)	16x Clock Frequency (KHz)	Origin
9,600	153.6	CNT9p6
4,800	76.8	CNT9p5
2,400	38.4	CNT9p3
1,200	19.2	CNT9p2
600	9.6	CNT9p4
300	4.8	CNT9p13
110	1.76	CNT8p6

Note that the 16x clock for the 110 baud rate is obtained by dividing the 1200 baud 16x rate by 11 with CNT8 and A6. A common problem that arises with the ACT-V I/O circuits is for the user to position the baud select switch in the null position. Be sure to refer to your operating manual to assist in selecting the data rate.

4.6 Bell Circuit

When the ACT-V receives a bell code (07 hex), completes a SEND or SHIFT SEND operation or removes the cursor from the screen in the hold screen mode it sounds an audible tone. The F8 causes a negative going pulse to appear at CR1p1 and N6p13. This pulse triggers the one-shot whose output at N6p11 gates the 16x 110 baud UART clock of 1760 Hz through A6p1 to Q10 which drives the speaker. The tone lasts for about one half of a second.

4.7 Printer Port

The unidirectional printer port of the ACT-V provides a serial RS232C output signal at pin 14 of the 25 pin I/O connector. Serial data out of the UART at U1p25 is routed through DS6p4 to R20 which is tied to the base of Q7. A high level (mark) at U1p25 and DS6p4 cuts off Q7 and I/O Conn p 14 is then pulled to -12 volts by R18. A low level at U1p25 and DS6p4 turns Q7 on and pulls I/O Conn p 14 high. When the F8 routes the serial data through DS6 to the printer output interface it also routes the printer baud rate clock from J2p15 to U1p17 and 40. Printer readiness is reported at I/O Conn p 24. Before transmitting each character during a PRINT operation the F8 samples this printer ready line and suspends transmission if it is low. If no connection is made to this pin the F8 will assume the printer is ready.

4.8 Current Loop Interface

The current loop interface consists of two full wave bridges and two optical isolators. When the ACT-V serial output at U1p25 is marking (High) CR2p2 is low, the LED in the optical isolator is on and causes the isolator transistor to conduct. This transistor combines with Q8 to form a Darlington pair which drives the full wave bridge such that current will flow in either direction through the AC inputs to the bridge. When the serial output is spacing (low) the LED in the optical isolator is cut off and no current will flow in either direction through the AC inputs of the bridge.

5. CPU - PROCESSOR CIRCUITS

The following integrated circuits are considered to be integral components of the microprocessor which controls and defines the ACT-V: CPU(F8 3850 microprocessor), SMI (3853 Static Memory Interface), MPB,MPT (Master Control Roms - 2708), CR1 (Control Rom 1), and the gates in N5 and N6.

Familiarity with microprocessor concepts and practices in general and those of the F8 in particular are helpful -- if not mandatory -- in understanding the discussion that follows. The interested reader should refer to the F8 Users Guide (published by Fairchild Semiconductor, a division of Fairchild Camera and Instrument Corporation, 464 Ellis Street, Mountain View, California 94042) for detailed descriptions of the F8 operation not included in this manual.

5.1 Data Bus Control

In order for the F8 to completely control the functioning of the ACT-V it is interconnected to the other circuits in a number of ways. These interconnections permit the F8 to perform the functions described in the following sections.

The principal channel of communication between the F8 and the other circuits in the ACT-V is the 8-bit bi-directional data bus. Devices connected to this bus are categorized as either drivers (sources) or receivers (sinks). Some devices possess both source and sink capabilities. Devices connected to the data bus and their capabilities are:

DEVICE	DRIVER	RECEIVER
F8-CPU	X	X
F8-SMI	X	X
RAM	X	X
I/O UART	X	X
MPB,MPT	X	

Selection of the data bus driver/receiver pair at any given time is controlled by the three most significant SMI address lines (A13, 14 and 15), CPU Read (SMIp34) and RAM Write (SMIp6). All of these signals provide inputs (addresses) to CR1. CR1 decodes these input signals and produces outputs under the circumstances given in Figure 5.1 and Table 5.1.

The next few paragraphs contain explanations of the actions caused by the eight outputs of CR1.

PIN 1:

A negative going pulse out of this pin triggers the one-shot whose output at N6p11 enables the 110 baud UART clock (1760 Hz) to drive the speaker and produce an audible beep when the ACT-V receives the Bell code or when block transmission to either the host computer or the local printer terminates.

PIN 2: $\overline{\text{Incr}}$ Row Offset Pointer (C6)

When the ACT-V scrolls all data in the RAM memory locations corresponding to the top row of the display is changed to an ASCII SPACE (code 20 Hex) and the Row Offset Pointer (ROP) is incremented. Incrementing the ROP causes the old second line to be displayed at the top of the screen while the old top line "moves" to the bottom of the display. Increment pulses from the F8 are OR-ed with those from the display circuit at OR1p8 and C6p1. Increment pulses from the F8 occur during the Horizontal retrace period and therefore do not collide with increment pulses from the display circuit.

PIN 3: $\overline{\text{Read}}$ Master Control ROMs (MPB,MPT)

The 2048 word Master Control ROMs of the ACT-V reside in the first 2k of the 65k address space of the F8. Any reference to these locations (0-7FF) by the F8 results in CR1p3 producing a negative going pulse that allows the MCR to drive the data bus. A10 is used in conjunction with CR1p3 to select either VB (0-3FF) or VT (400-7FF).

PIN 4: $\overline{\text{Read}}$ Display RAM

This line goes low to enable the Display RAM to drive the F8 data bus. This takes place each time a displayable character is received by the I/O UART and read into the F8. First the location pointed to by the cursor is loaded with the received character and a low (off) cursor bit. Then the next position to be pointed to by the cursor is read in and written back with a high (on) cursor bit. The display RAM is also read during SEND and PRINT operations.

PIN 5: $\overline{\text{Write}}$ to RAM

A negative going pulse on this line causes the data placed on the F8 data bus during the execution of an F8 STORE instruction to be loaded into the display RAM in the location specified by the F8 Data Counter. F8 access to the display RAM is restricted to Horizontal and Vertical Sync periods. Hence the display RAM appears to have a 64 usec access time to the F8.

PIN 6: $\overline{\text{Read}}$ I/O UART

A negative going pulse here causes the I/O UART to drive the F8 data bus with the contents of its receiver holding register. This operation is performed each time the I/O UART receives a character and the F8 reads it.

PIN 7:

This line, in conjunction with the "blank the display line" at CPUp10 and the dot oscillator enable line (FF1ap12), controls the address multiplexer to the display RAM (DS1,2,3). This line is asserted whenever the F8 reads or writes data from or to the RAM.

PIN 9: $\overline{\text{Write}}$ to UART

This line in conjunction with Bit 0 of I/O port 1 controls transmission of parallel data to the UART. The write pulse emanating from CR1p9 drives the multiplexer on the Data Strobe ($\overline{\text{DS}}$) line of the transmitter in the I/O UART. The LSB of I/O Port Ø in the F8 (CPUp16) is tied to the select lines of the

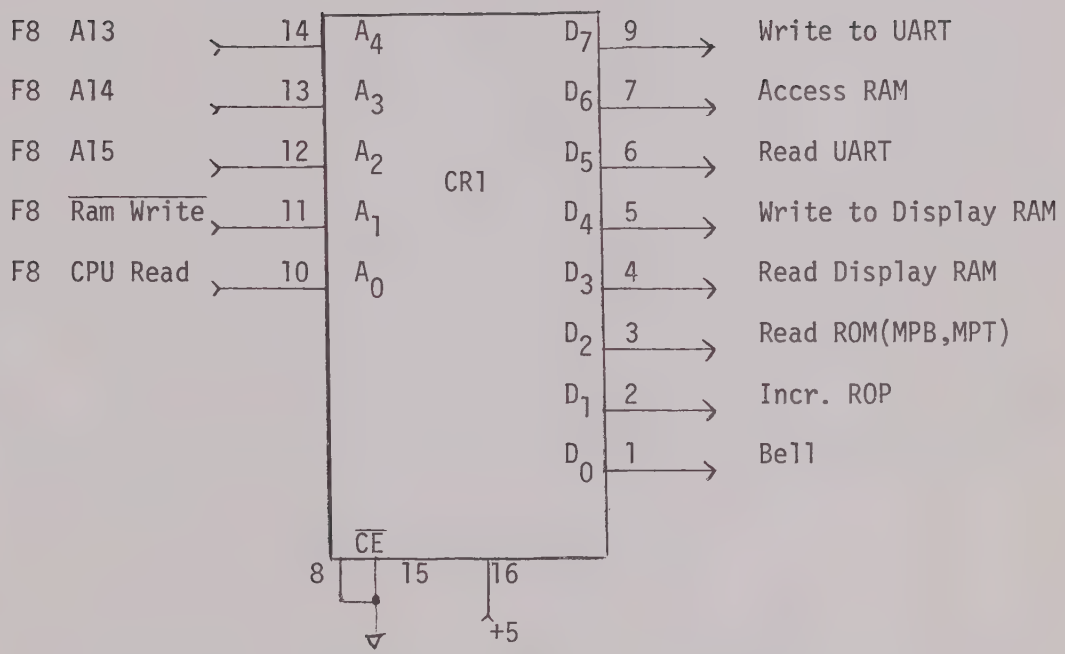


Figure 5.1: CR1 Connections

	INPUTS to CR1				OUTPUTS OF CR1								
OPERATION	SMI A13	SMI A14	SMI A15	RAM $\overline{\text{WRITE}}$	CPU READ	$\overline{\text{WRITE}}$ TO UART	ACCESS RAM	$\overline{\text{READ}}$ UART	$\overline{\text{WRITE}}$ TO RAM	$\overline{\text{READ}}$ RAM	READ MP (Bor T)	INCR CNT 6	$\overline{\text{RING}}$ BELL
Read MP(Bor T)	0	0	0	1	1	1	0	1	1	1	1	0	1
Ring Bell	1	1	1	0	0	1	0	1	1	1	0	0	0
Read RAM	0	1	0	1	1	1	1	1	1	0	0	0	1
Write to RAM	0	1	0	0	0	1	1	1	0	1	0	0	1
Read UART	0	0	1	1	1	1	0	0	1	1	0	0	1
Write to UART	0	0	1	0	0	0	0	1	1	1	0	0	1
Incr CNT 6	1	0	0	0	0	1	0	1	1	1	0	1	1
NONE	ALL OTHERS					1	0	1	1	1	0	0	1

Table 5.1: Inputs and Outputs of CR1

multiplexers feeding data and strobe signals to the I/O UART's transmitter. When the F8 raises this line high write pulses to the UART will load the data on the F8 data bus into the UART for transmission to either the host computer via pin 2 of the EIA I/O connector or to the printer via pin 14 of the EIA I/O connector. This line is normally low when the ACT-V is in the (on) LINE mode. Hence the keyboard drives the UART transmitter unless the ACT-V receives a request for cursor position. Receipt of this code causes the F8 to take control of the I/O transmitter by raising CPUpl6 while transmitting the values of the row and column counters. In the LOCAL mode the select line from CPUpl6 remains low until the SEND key is depressed on the keyboard. The F8 then takes control of the I/O transmitter while sending data out the RS232C interface to pin 2 of the EIA connector. During this period the ACT-V's Data Terminal Ready (DTR) line at pin 20 of the I/O connector is held low to indicate that it is busy transmitting data and is ignoring characters received at the UART until the transmission is complete.

5.2 CPU I/O Port Assignments

The F8 uses its two 8-bit bi-directional I/O ports to observe and control the state of the ACT-V. A description of the electrical characteristics of the F8 I/O ports can be found in the F8 Users Guide published by Fairchild. The I/O port assignments and a description of their uses are as follows:

5.2.1 I/O Port Ø

Bit Ø (CPUpl6): UART Transmitter select. This line controls whether the keyboard or the F8 drives the UART transmitter buffer. A high level selects the F8 and a low level selects the keyboard.

Bit 1 (CPUp11): Intensity Bit to RAM. This line provides the intensity information to the display RAM when characters are written to it. A high level indicates full intensity (unprotected data) and a low level indicates half intensity (protected field). Intensity information is read back from the display RAM to the F8 on the MSB of the data bus.

Bit 2 (CPUp10): Display Blanking. When this line goes low the video output to the CRT is blanked. This is done when the F8 performs operations that require display RAM access at times other than during horizontal retrace (add or delete a line are two examples).

Bit 3 (CPUp5): DTR. This line drives pin 20 (Data Terminal Ready) of the 25 pin I/O connector through an Operational Amplifier (OA2) to indicate readiness on the part of the ACT-V to accept data. This line goes low during a SEND or PRINT operation and remains high otherwise.

Bit 4 (CPUp36): Transmitter Buffer Empty/End of Character (TBE/EOC). This line is pulled low by the UART when it is busy transmitting a character. The F8 senses this and suspends transmission of characters to the UART until it returns high.

Bit 5 (CPUp31): UART Select. This line controls the multiplexer (DS6) that routes either the I/O baud rate clock (from B.R.S.1) or the printer baud rate clock (from J2p15) to the UART clock pins (40 and 17). It also routes the UART serial output (from U1p25) to either the printer output at I/O connector pin 14 (via R20 and Q7) or to pin 14 of the I/O control rom (CR2). If the ACT-V is in the LINE mode the serial data emerges at CR2p4 and drives I/O connector pin 2 (RS232 data out) through Op. Amp 2. The UART select line also chooses either the Data Set or printer ready lines to pass on to CPUp7 -- see description below.

Bit 6 (CPUp30): Terminal Option Switch 3. This line reports the status of T.O. Sw. 3 to the F8. When low (T.O Sw. 3 = 0) the selected terminal is not enhanced. When high the terminal selected is enhanced.

Bit 7 (CPUp25): Display Column Address 7. This input line is sampled by the F8 to detect the advent of the horizontal sync pulse.

5.2.2 I/O Port 1

Bit Ø (CPUp27): Character Origin. This input line is driven by FF3p13 to indicate whether the most recently received character was from the ACT-V or from the remote computer.

Bit 1 (CPUp13): Reset Row Offset Pointer. During the power on sequence this line is pulsed low when the F8 senses the display has entered the display-off period prior to the start of the next vertical scan. This pulse is inverted at N4p11 and applied to the reset line of Cnt 6 (p2). Resetting the Row Offset Pointer in this manner establishes an agreement as to the row address of the first line of characters between the display and loading circuits.

Bit 2 (CPUp8): Terminal Option Switch 2. This line reports the position of T.O. Sw. 2 to the F8 to allow it to determine the type of terminal desired.

Bit 3 (CPUp7): Computer/Printer Ready. This line is driven by DS6p7 which is the translated ready signal. A high level at CPUp7 indicates readiness on the part of the computer or printer to accept data.

Bit 4 ($CPUp_{34}$ Not Used.

Bit 5 (CPUp33): Terminal Option Switch 1. This line reports the position of T.O. Sw. 1 to the F8 to allow it to determine the type of terminal desired.

Bit 6 ($CPUp_{28}$ Not Used.

Bit 7 (CPUp14): Display Enable. This input line is driven by the Display Enable signal and is sampled during the power on sequence to initiate a reset pulse to the Row Offset Pointer (Cnt 6) as described in the paragraph titled Bit 1 above.

6. SYNCHRONIZATION GENERATION CIRCUITS

The synchronization generation circuits of the ACT-V are responsible for producing horizontal and vertical sync signals to drive the CRT display and various other internal synchronizing signals. All of these signals are generated from a single master oscillator.

6.1 Dot Oscillator and Counter

The master oscillator is referred to as the dot oscillator and has a frequency of 9.828 MHz.

The dot oscillator is a ring oscillator whose output frequency (at N1p8) is determined by the crystal inserted between N1p6 and N1p1. The dot oscillator output drives CNT1 -- the modulo-six dot counter. Every sixth dot, as N1p8 falls, CNT1p9 and CNT1p8 rise forcing A1p6, N2p5 and N1p12 high. When N1p8 rises, (one half cycle of the dot oscillator later) a negative going pulse with duration equal to half of a dot oscillator cycle is fed to the count-up input line of CNT2 (CNT2p5 through N1p11).

6.2 Horizontal Position Character Counter (CNT2, CNT3) - Display Column Counters

CNT2 and CNT3 count the number of character positions in a horizontal scan. An ACT-V has 105 character positions per horizontal scan. The ACT-V displays characters in 80 of these positions. The remaining positions correspond to left and right horizontal margins and the horizontal sync interval. Table 6.1 on the next page shows the allocation of character positions as counted in CNT2 and CNT3.

CNT2, CNT3 Contents	ACTION
2	Begin displaying characters (Gate the dot oscillator to the video generator) End the left margin
82	Cease displaying characters (Quit sending pulses to the video generator) Begin right margin
84	Start horizontal sync interval End right margin
105=0	End horizontal sync interval Begin left margin NOTE: There is a 2 character wide left margin on the ACT-V display.

Table 6.1

The outputs of the character position counter (Display Column Counter) are:

BIT #	SIGNIFICANCE	ORIGIN
DCØ	1 (LSB)	CNT2p3
DC1	2	CNT2p2
DC2	4	CNT2p6
DC3	8	CNT2p7
DC4	16	CNT3p3
DC5	32	CNT3p2
DC6	64	CNT3p6

DC2 through DC6 are used to address Control ROM 3 (CR3). Signals generated by CR3 and N3 control the Dot Oscillator Enable flip-flop (D.O.En.-FF1a) and FF1b and also provide the horizontal sync pulses for the direct-drive data display monitors.

The modulo 105 operation of CNT2 and CNT3 in a ACT-V is achieved by pulling low on the $\overline{\text{Load}}$ inputs of CNT2 and CNT3 (CNT2, CNT3p11) when the column count reaches 104 and N3p8 goes low. Timing diagrams for the functions which operate at the horizontal frequency are provided in Figure 6.1.

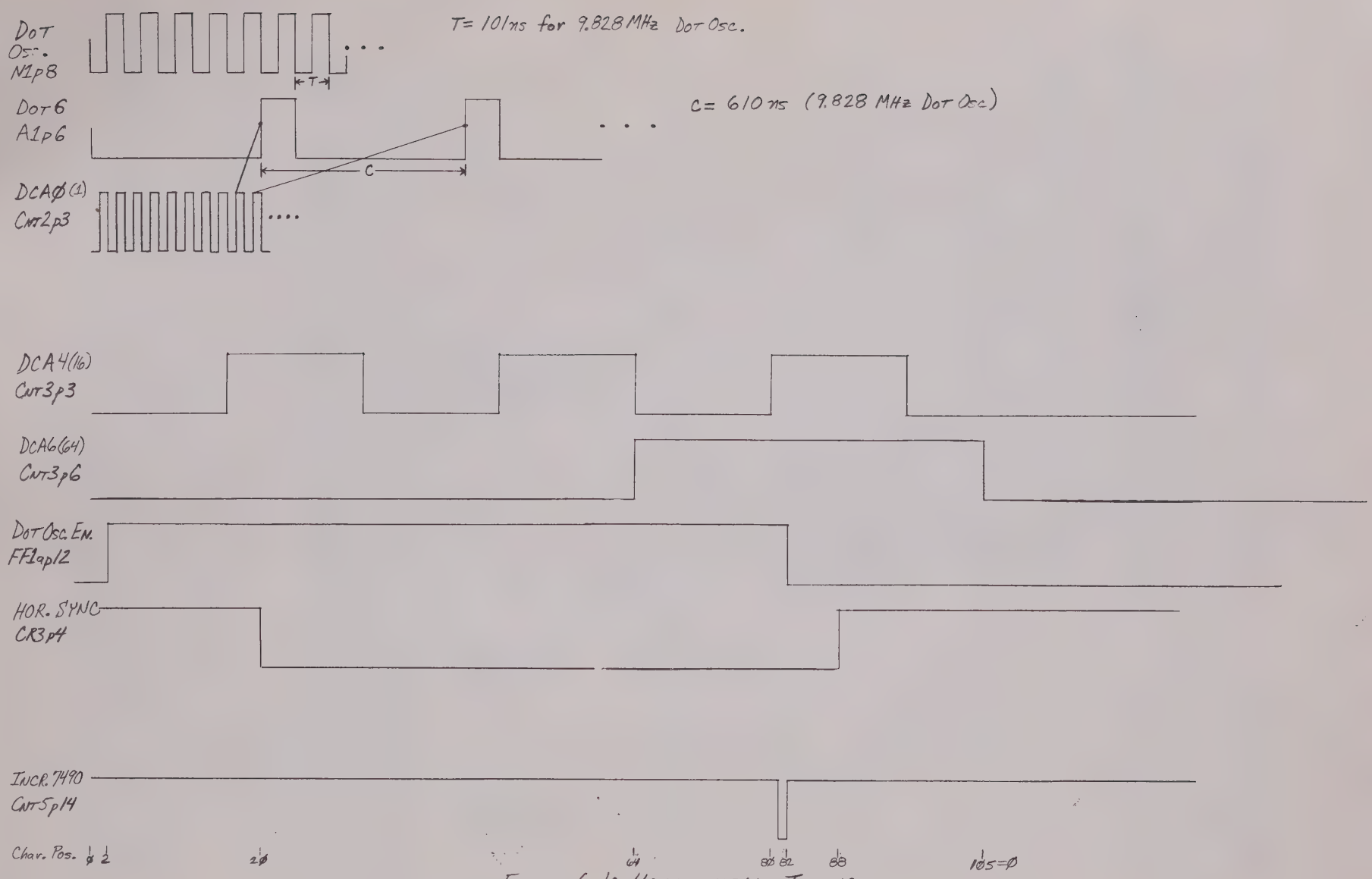


FIGURE 6.1: HORIZONTAL TIMING

6.3 Dot Oscillator Enable Flip-Flop

The clock line of the D.O.En. flip-flop (FF1ap1) is pulsed when C2p2 (DC1) goes high and CNT3p6 (DC6) is low. The J and K inputs of the D.O.En. flip-flop are tied to the Q and $\overline{Q}$ outputs of the Display Enable flip-flop (Disp. En.-FF2a). Hence the clock pulses at the D.O.En. flip-flop cause it to be set only when the Disp. En. flip-flop is set -- i.e. the beam is vertically positioned in the display area. Operation of the Disp. En. flip-flop is described in Section 6.5 below. When the D.O.En. flip-flop sets its Q output allows the negative going strobe pulses that occur during the second half of every sixth dot to pass from N2p6 to the shift-register (SR1) and to the data latches (L1, L2) in the video generator (VG) circuit. The high Q output of the D.O.En. flip-flop also permits the shift pulses that occur during the second half of every dot to pass from A1p8 to SR1p7 and gates cursor and video data in the video generator circuit as described in Section 8. When the Display Column Counters (CNT2, CNT3) reach a value of 82 (80 characters after the D.O.En. flip-flop was set) a negative going pulse is applied to the reset pin of the D.O.En. flip-flop and it resets -- pulling its Q output low and disabling all functions it had enabled. When the Display Column Counters (CNT2, CNT3) reach a count of 81 (as the beam finishes passing through the sixth dot of the 79th horizontal display position) an increment pulse is sent from FF1bp8 to CNT5p14. CNT5 is a modulo ten character scan line counter whose operation is described in Section 8.

6.4 Horizontal Sync. Generation

Horizontal sync. pulses begin at a column count of 88 and end at a count of 20. Since CNT2 and CNT3 are modulo 105 counters the direct-drive Hor. Sync. pulses for the 12 inch data-display monitor last for 40 character positions. This Hor. Sync. output is routed to the monitor through P4p1 to V.Con p6 and Mon p6.

6.5 Vertical Sync and Display Enable Generation

A nine bit scan line counter (CNT4) is used to count horizontal sync pulses and thus indicate the vertical position of the beam in the same manner that the Display Column Counters CNT2 and CNT3 count character positions to indicate the horizontal position of the beam. Figure 6.2 provides a pictorial representation of the timing functions described below. The count in line of CNT4 at pin 10 is driven by CR3p3. CNT4 is reset at the beginning of the vertical sync (Vert. Sync.) interval and at a given instant its outputs indicate the number of horizontal sync pulses that have occurred since the start of the most recent Vert. Sync. pulse. The outputs of CNT4 are decoded to control the Vert. Sync. flip-flop (FF2b) and the Display Enable flip-flop (FF2a). A summary of the operation of these flip-flops for both 60 Hz and 50 Hz models is given in the following table:

MODEL	(60 Hz)	(50 Hz)
Set Disp. En. FF	16	16
Reset Disp. En. FF	256	256
Set Vert. Sync. FF	260	312
Reset Vert. Sync. FF	5	5
Reset CNT4	260	312

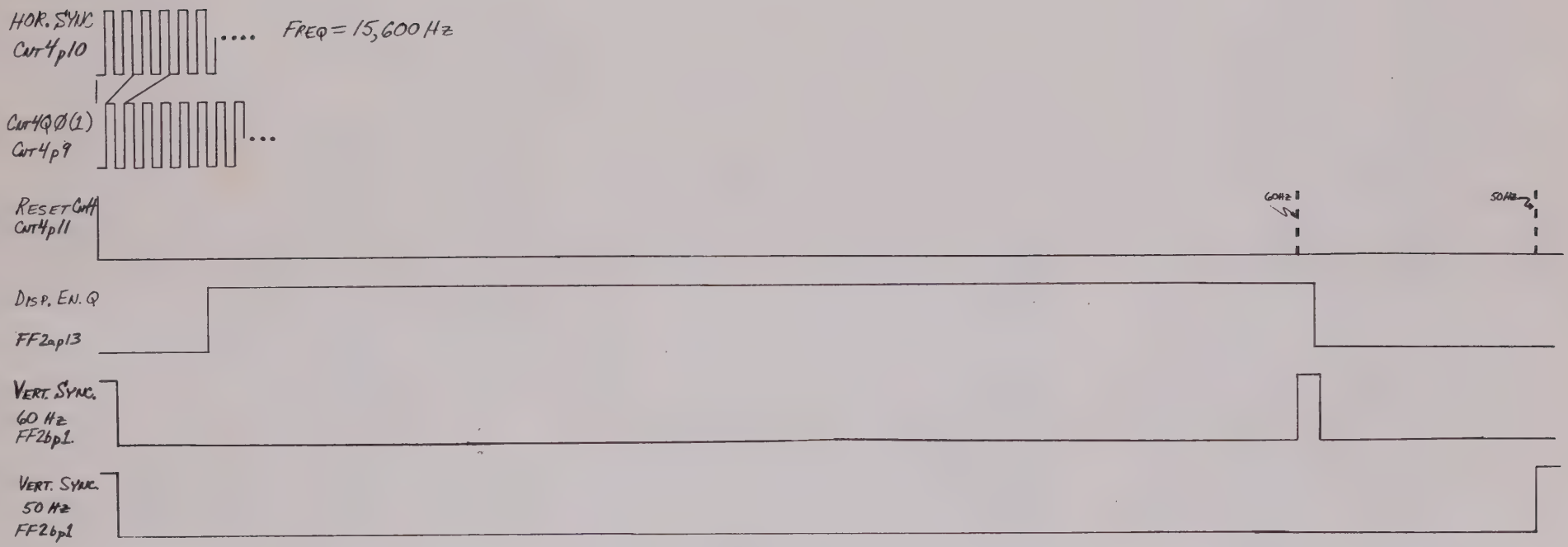
Using the information provided in the foregoing tables and knowing the dot-oscillator frequency, one can calculate the Vert. Sync. frequency using the equation:

V.Sync. Freq. = Dot Osc. Freq. ÷ 6 ÷ Modulo of CNT2,CNT3 ÷ modulo of CNT4.

Plugging in values for the ACT-V we obtain:

V. Sync. Freq. =

$$\frac{9.828 \times 10^6}{6 \times 105 \times 260} = 60.00 \text{ Hz}$$



Scan Line 1 2 4 5 16 24 220 240 256 260 264 266 Ø 300 312

FIGURE 6.2: VERTICAL TIMING

A Vert. Sync. rate of 50 Hz can be achieved by changing the modulo of CNT4 from 260 to 312. This is accomplished by selecting alternate inputs to the gating circuits that control the Vert. Sync. and Disp. En. flip-flops.

The set pulse to the Disp. En. FF is delayed until horizontal scan line number 16 to allow for a margin at the top of the screen. Negative Disp. En. at FF2ap12 drives an I/O port line of the F8 (CPUp27).

$\overline{\text{Vert. Sync.}}$ at FF2bp2 drives the $\overline{\text{V. Syn.}}$ input at pin 9 of the monitor connector.

6.6 Row Offset Pointer - CNT6

The last portion of the Sync. Generator (SG) circuits is the Row Offset Pointer (ROP) CNT6. This counter points to the row of characters in memory to be displayed in the first row on the screen. CNT6 is a modulo 24 counter that increments each time the display circuitry finishes displaying a row of characters (i.e., the beam passes through the 10th row of dots in the 80th character and the D bit of CNT5 falls) or when the load circuit performs a scroll operation. The F8 issues scroll pulses only when CNT6 is not being incremented by the display circuits. This prevents CNT6 missing any counts and losing sync. As described in Section 5, during a power-on sequence CNT6 is reset by the F8 and the F8's internal pointer to the row of memory that is to be displayed at the top of the screen (first row) is also set at zero. If for any reason (such as voltage spikes on the power line) these two pointers become unequal, the ACT-V will incorrectly position the cursor in a row other than the top one when commanded to move to the home position. The two pointers can easily be resynchronized by turning the ACT-V off and back on immediately (forcing a power-on restart).

7. REFRESH RAM

The refresh RAM stores the 7 bit ASCII codes for the characters to be displayed on the ACT-V monitor. It also has storage to position the cursor and to determine whether the characters are to be displayed in full or half intensity. The memory capacity is 2048 words of 9 bits (7 ASCII, 1 cursor, 1 intensity). Only 1920 locations are accessed by the ACT-V for display purposes (24 lines by 80 characters).

7.1 Addressing

In general, 11 bits of address are required to uniquely address 1920 memory locations. The ACT-V memory is addressed by 12 bits -- 5 bits to encode the row address (0-23) and 7 bits to encode the column address (0-79). Both the memory loading circuitry and the display generation circuitry retain their own copies of these address. These two addresses are presented to the 12 bit digital switch comprised of DS1, DS2 and DS3. Row and column address bits for the display and load circuit inputs to the digital switch and the selected outputs can be found at the following pins on DS1, 2 and 3:

ADDRESS LINE NAME	ORIGIN	SWITCH CONNECTION	SELECTED OUTPUT	NAME
Column Addressing				
Display Column Address LSB (DCAØ)	CNT2p3	DS1p14	DS1p12	CAØ
Load Column Address LSB (LCAØ)	SMIp15	DS1p13		
DCA1	CNT2p2	DS1p2	DS1p4	CA1
LCA1	SMIp14	DS1p3		
DCA2	CNT2p6	DS1p5	DS1p7	CA2
LCA2	SMIp13	DS1p6		
DCA3	CNT2p7	DS1p11	DS1p9	CA3
LCA3	SMIp12	DS1p10		
DCA4·$\overline{OVF}$	A3p6	DS2p5	DS2p7	CA4
LCA4	SMIp11	DS2p6		
DCA5	CNT3p2	DS2p11	DS2p9	CA5
LCA5	SMIp10	DS2p10		

ADDRESS LINE NAME	ORIGIN	SWITCH CONNECTION	SELECTED OUTPUT	NAME
DCA5·$\overline{OVF}$	A3p3	DS2p14	DS2p12	CA6
LCA6	SMIp9	DS2p13		
Row Addressing				
Display Row Address LSB (DRAØ)	C6p12	DS3p2	DS3p4	RAØ
Load Row Address LSB (LRAØ)	SMIp25	DS3p3		
DRA1	C6p11	DS3p14	DS3p12	RA1
LRA1	SMIp26	DS3p13		
DRA2	C6p9	DS3p11	DS3p9	RA2
LRA2	SMIp27	DS3p10		
DRA3	C6p6	DS2p2	DS2p4	RA3
LRA3	SMIp28	DS2p3		
DRA4	C6p5	DS3p5	DS3p7	RA4
LRA4	SMIp29	DS3p6		

The 6th and 7th bits of the display column address (DCA4 and DCA6) are obtained by anding the overflow ($\overline{OVF}$) output of CR3 (CR3p6) with the 6th and 7th bits of the modulo 105 character space counter. This results in a modulo 80 display column address.

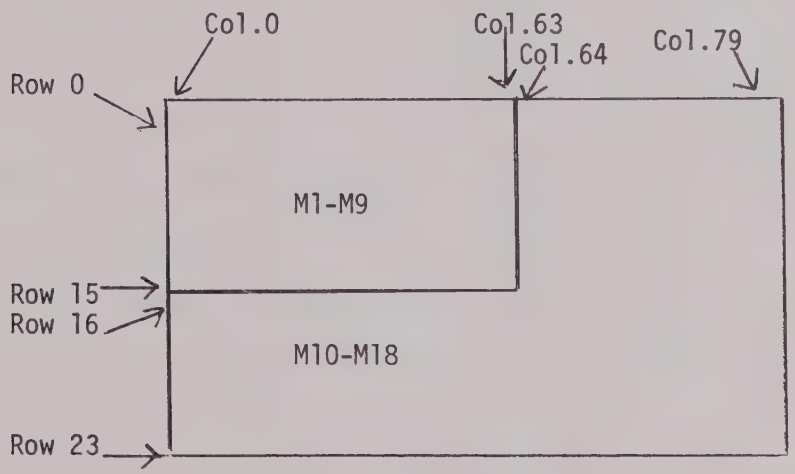
The 12 bit output of digital switches DS1, 2 and 3 needs to be mapped into an 11 bit address to access the refresh RAM. This mapping is performed by 2 And gates (A3) and 3 Or gates (OR1). The 7 column address bits (CAØ-CA6) and the 5 row address bits (RAØ-RA4) are mapped into the 11 memory address bits (MAØ-MA10) as follows:*

SELECTED COLUMN or ROW ADDRESS or OTHER GATE FUNCTION	ORIGIN	MEMORY CONNECTION
CAØ	DS1p12	M1-M18p15
CA1	DS1p4	M1-M18p16
CA2	DS1p7	M1-M18p14
CA3	DS1p9	M1-M18p2
CA4 + (CA6·RA4)	OR1p3	M1-M18p4
CA6	DS2p12	M1-M9p1
CA5 + (CA6·RA3)	OR1p6	M1-M18p5
RAØ	DS3p4	M1-M18p7
RA1	DS3p12	M1-M18p6
RA2	DS3p9	M1-M18p8
RA3	DS2p4	M10-M18p1
$\overline{RA4 + CA6}$	OR1p11	M1-M9p13 ($\overline{CE}$)
$\overline{RA4 + CA6}$	N4p6	M10-M18p13 ($\overline{CE}$)

* + indicates the logical OR function; · indicates the AND function

This address assignment divides the screen into two portions: One portion is stored in M1-M9 and is selected when the column address is in the range 0-63 and the row address is between 0 and 15 (decimal) inclusive. The other half of the memory (M10-M18) is selected when either CA6 is high (column count of 64 to 79) or RA4 is high (row address of 16 to 23).

When the row offset counter C6 has a value of zero the allocation of memory sections to the display looks like



The above pattern rolls upward (i.e., the top row replaces the bottom row and all others move up once) each time the ACT-V performs a scroll operation and C6 is incremented.

7.2 Data Bus Interfacing

The ACT-V refresh RAM is connected to the F-8 data bus through an 8 bit tri-state buffer (B1). When the processor wants to write data into the RAM the 7 bit ASCII code and the cursor bit are placed on the F-8 data bus while the intensity bit is present at the F-8 I/O port. The relationship between F-8 data bus bits and memory chips is as follows:

SIGNAL NAME	F-8 DATA BIT #	MEMORIES USED
ASCII BIT 1	B0	M1, 10
ASCII BIT 2	B1	M2, 11
ASCII BIT 3	B2	M3, 12
ASCII BIT 4	B3	M4, 13
ASCII BIT 5	B4	M5, 14
ASCII BIT 6	B5	M6, 15
ASCII BIT 7	B6	M7, 16
CURSOR BIT	B7	M9, 18
INTENSITY BIT	I/O PORT 0 BIT 1	M8, 17

When the F-8 needs to read from a location in the refresh RAM the data bus control circuit produces an enable pulse from CR1p4 to B1p19 while addressing the desired location. This enable pulse causes the addressed data to drive the data bus through B1.

When either writing to or reading from the refresh RAM the RAM driver select line at DS1, 2 and 3p1 is driven by the processor circuit to select the load column and row addresses for driving the memory. This line is returned low to allow the display circuits to address the RAM.

8. VIDEO GENERATOR CIRCUIT

The Video Generator (VG) circuit of the ACT-V receives parallel ASCII data from the refresh RAM and sync signals from the sync generator and produces video signal(s) capable of driving the direct-drive data display monitor in the ACT-V.

8.1 Character Font

The ACT-V display is sectioned into 1920 character positions in a 24-line by 80 column grid of 6 x 10 dot matrices. A basic character position is illustrated in Figure 8.1 below. Both row 0 and column 6 are always blank to provide a boundary between characters. Rows 8 and 9 are used only by descending lower case letters and the cursor. A complete listing of the character generator ROM is given in the Appendix. Ten address lines are required to indicate the character (7 bits of ASCII) and the character scan line (3 bits) to be displayed. Latches L1 and L2 provide the 7 ASCII data bits and CNT5 -- the Modulo 10 character scan line counter provides the 3 bits needed to indicate which scan line is to be displayed. These address lines are summarized in Table 8.1.

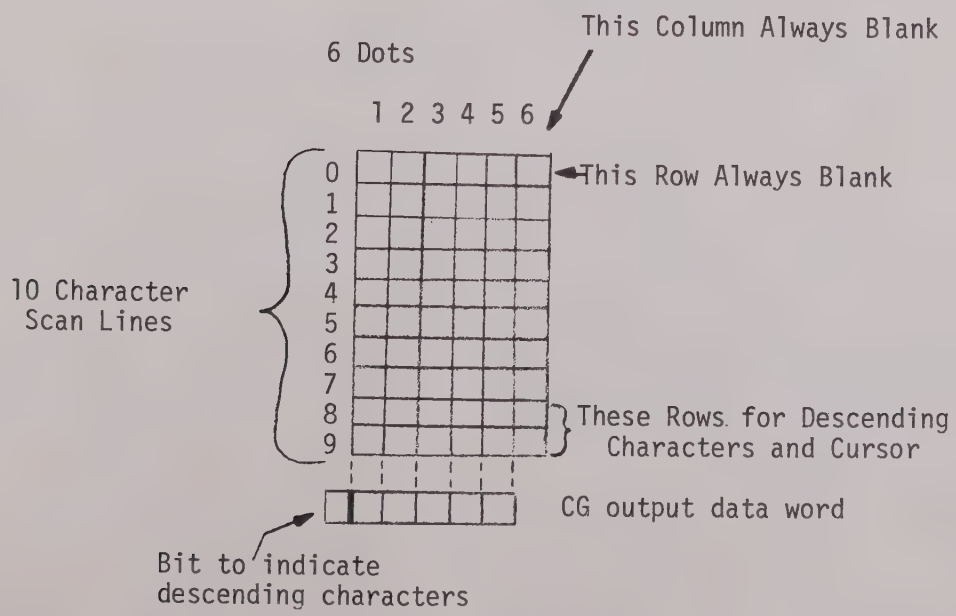


Figure 8.1: Individual Character Grid

Source	Address Bit to CG
ASCII Bit 1	0
" " 2	1
" " 3	2
" " 4	3
" " 5	4
" " 6	5
" " 7	6
CNT5 Bit A (LSB)	7
CNT5 Bit B	8
CNT5 Bit C (MSB)	9

Table 8.1: Character Generator Addressing

An example of how a particular character's dot pattern is stored in the CG ROM is as follows: Suppose we take the character A (ASCII code 41 Hex) for example. The dot pattern for its first row (ROW Ø) can be found in location 041 of the CG. Referring to the listing provided in the Appendix we see that the data in location 041 is 00 (Hex). This causes row 0 of the letter A to be blank. By incrementing CNT5 by one we find that the CG address for the row 1 dot pattern is 0C1. The data at this address is 04. Since the output data word corresponds to the character dot positions as shown in Figure 8.1 output word 04 causes dot 3 to be turned on at the top of the A. This process can be repeated with the following results:

Scan line	CG Address	Data	Dot Pattern
1	0C1	04	o o ● o o
2	141	0A	o ● o ● o
3	1C1	11	● o o o ●
4	241	11	● o o o ●
5	2C1	1F	● ● ● ● ●
6	341	11	● o o o ●
7	3C1	11	● o o o ●

Using the information provided above one may design his own character set.

8.2 Display Sequencing

Each time the beam passes through the sixth dot of a display position (anywhere in the 24 x 80 grid) N2p6 pulses low and jams the dot pattern of the present scan line of the next character to be displayed into the shift register (SR).

At the same instant the ASCII code and the cursor and intensity bits for the next character (next here meaning the one to be displayed after the one in the shift register) are loaded into the latches L1 and L2 and the character generator (CG) begins looking up the dot pattern for that character. This dot pattern is to be loaded into the shift register when the beam passes through the next sixth dot. Figure 8.2 illustrates this procedure. Suppose the beam is passing through the top scan line of the letters ABC. The sixth dot pulse generated between the A and B jams the dot pattern for the first row of the letter B (11110) into the shift register while simultaneously loading the ASCII code 43 (Hex) with a high cursor bit into the latches. As soon as this code appears at the outputs of the latches the character generator ROM starts looking up the dot pattern for the top row of the C (01110). This data is jammed into the shift register as the beam passes through the sixth dot in the top row of the B.

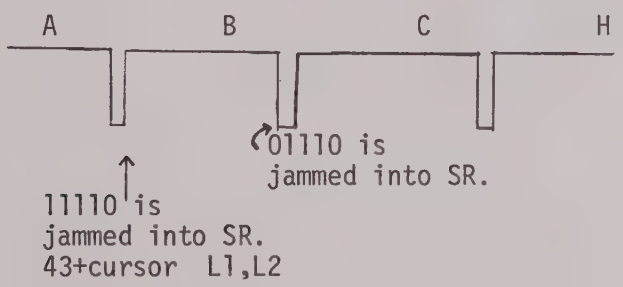


Figure 8.2: Display Sequencing

This type of display sequencing resembles a bucket brigade since the character generator is always looking up data for the next character to be displayed (i.e. the CG is one character ahead of the video output) and the display RAM is accessing data for the second character to be displayed after the present one (i.e. it is two characters ahead of the video).

8.3 Video Signal Composition

Digital dot pattern data shifted out of SR at pin 13 is anded with the dot oscillator enable flip-flop, the blank the display signal (CPUp10) and the signal produced at XORp6. This signal falls and prevents rows 0 and 1 from being displayed until rows 8 and 9 when the character is a descending lower case one. When non-descending characters are displayed XORp6 pulls low and prevents the recurrent display of row 0 and 1 during rows 8 and 9. Anding SRp13 with the dot oscillator enable flip-flop and the CPU display blanking signal at A2p6 prevents video data from being displayed outside of the 24 x 80 display area or during F8 memory access periods. The cursor enable at L2p12 is also anded with the dot oscillator enable FF and the CPU display blanking signal at A2p8. Digital video data at A1p3 is summed into the video combiner circuit along with a duplicate signal from A5p3 (for full intensity characters) and cursor data from A2p8. The summing point for the video output is the base of Q1. Q1 is an emitter follower circuit that provides a low impedance video signal to drive the internal monitor.

9. TROUBLESHOOTING

This section contains a list of trouble symptoms, their causes and remedies. It also describes the disassembly procedures for the ACT V.

SYMPTOM	CAUSE	REMEDY
Dark horizontal band slowly rolls up screen.	One of the two diodes in the +5v full wave bridge bad and causing ripple on +5.	Replace defective diode.
All keys work except one.	Bad key or loose solder connection to that key.	Visually inspect key and solder joints.
No keyboard strobe pulses at J1p1.	Either a keyswitch is stuck down or shorted or OS1, DS1, 2 or CNT1 is bad.	Free jammed key or replace defective IC.
No characters displayed yet cursor moves when loading characters.	Defective C.G. or S.R.	Determine IC at fault and replace.
Character(s) appear on screen at positions not containing cursor while loading at cursor.	Crosstalk in one of M1-M18.	Determine faulty bit (by comparing extra characters ASCII code to space code -Hex 20) and replace memory chip.

9.1 Troubleshooting Hints

To perform any diagnosis and/or repair work on a ACT-V terminal you should have thoroughly familiarized yourself with the principles of operation described in the earlier sections of this manual. The following paragraphs suggest tests to perform to determine the cause of a malfunction in the various ACT-V circuits.

9.1.1 Keyboard Fault Diagnosis

If when you hold a selected key down on the keyboard you either (1) do not observe a strobe pulse at J1p1 or (2) note that the ASCII data at J1p2-8 is in error, then the keyboard circuits have failed. Roughly speaking, data failures are the result of MKE failing or DS4 or DS5 loading down the data lines. Strobe problems are usually due to a faulty OS1, N2, DS1 or DS2 chip. Refer to Section 3 of this manual for a detailed description of the keyboard circuits.

9.1.2 I/O Fault Diagnosis

If either (1) no serial data is present at pin 2 of the 25 pin I/O connector when both strobe and data signals from the keyboard are present, or (2) no serial data is present at U1p20 when the same is present at pin 3 of the 25 pin I/O connector the I/O circuit is malfunctioning.

When testing the output circuit one should verify that strobe, data and clock signals are present at the appropriate pins on the UART. Next check to see that the serial data out of U1p25 passes through to CR2p4 (when in remote) and drives OA2. Note that if for some reason CR2p11 does not get pulled up by the LINE/LOCAL switch no serial data will appear at I/O Conn. p 2.

9.1.3 Sync Generation

Troubles in the sync circuits can be due to either (1) the main oscillator quitting; (2) the divide by 6 counter CNT1 malfunctioning; (3) the character position counters CNT2 and CNT3 malfunctioning; (4) a faulty scan line counter CNT4; (5) a bad character row counter CNT6 or defective gates and flip-flops that provide the dot oscillator, horizontal and vertical sync signals. To identify the faulty circuit refer to Section 6 of this manual. Note that since CNT3p6 feeds CPUp25 if the CPU fails such that CPUp25 gets pulled high or low it will appear as if CNT3 is faulty when it is not.

9.1.4 Refresh RAM Diagnosis

The most common failure mode for the semiconductor memories used in the ACT-V refresh RAM is indicated by one or more characters appearing (or being altered) in positions other than the cursor position when loading characters at the cursor position. The faulty memory may be identified by noting that the ASCII code for the character that was altered usually differs from the ASCII code for the character that replaced it by only one bit. That reduces the possible candidates for the bad IC to only two memory chips (i.e., the two that store the bit in question). After

replacing these chips the malady should disappear.

9.1.5 Testing the Video Generator Circuits

In order to troubleshoot the video generator circuit you should study Section 8 of this manual.

If the cursor moves around on the screen when data is sent to the ACT-V but no characters are displayed either the character generator (C.G.) or the shift register S.R.) has failed.

9.2 Disassembly

Unplug the unit to gain access to the main logic board as follows:

Remove the five Phillips head screws that secure the top of the cabinet. The unit may now be plugged in for servicing.

9.2.1 Board Removal

Before attempting to remove the board, unplug the unit. The main logic board is mounted in the ACT-V with three brackets. Two of these hold the bottom of the board in place and the third stabilizes the top of the logic board by tying it to the monitor mount. To remove the main logic board, free it from these brackets and unplug S1, 2, 3, 4 and the ribbon connectors at J1 and J2. Be sure these connectors are all replaced properly before plugging the unit back in and applying power.

November 1, 1978

APPENDIX 1

ACT-V MAIN LOGIC BOARD PARTS LIST

Integrated Circuits

Part	Description	Quantity	Board Location
A1,2,3,5	74LS08	4	H3,I3,F4,J3
A4	4081	1	G3
A6	4082	1	I8
B1	81LS95	1	C7
CNT 1	7492	1	H2
CNT 2,3	74LS193	2	F2,F3
CNT 4,9	4040	2	G2,G8
CNT 5	7490	1	G5
CNT 6,8	4024	2	F5,H8
CNT 7	7493	1	J2
CG1	2708P	1	I5
CPU	3850	1	D6
CR 1,2,3	74S288	3	B2,B7,G2
DS1,2,3,4,5,6	74LS157	6	E2,E3,E5,A4,B4,A6
FFL,3	74LS73	2	G4,A1
FF2	4013	1	H4
FWB 1,2	VMØ8	2	A8,A8
ISO 1,2	4N37	2	A7,A7
L1,2	74LS174	2	J5,J4
M1-M18	2102L1PC	18	E6-K6 and E7-K7
MPB,MPT	2708P	2	C1,C2
N1	7400	1	I2
N2,3,4	74LS00	3	H4,G3,G5
N5,6	4011	2	A2,A2
OA1	UA1458TC	1	L5
OA2	LM348	1	B8
OR1	74LS32	1	E4
SM1	3853	1	D4
SR1	74166	1	H5
U1	AY5-1013	1	B4
X-OR1	74LS86	1	I4
	TOTAL	69	

ACT-V MAIN LOGIC BOARD PARTS LIST

Capacitors

Part # (Name)	Description	Quantity	Location
C1	4,700uf,25v	1	M2
C2	470uf,40v	1	L2
C3	2,200uf,25v	1	L4
C4,7,8,9,23,24	15uf,16v Tantalum	6	K1,M7,M6,J8,A2,B6
C5,10,11,12,13,14,18,19 20,25,26	.1uf ceramic	11	G6,I6,C8,C8,K2,F1, G1,G1,H1,I1,F6
C6,17,27	220pf silver mica	3	J2,G5,H4
C15	.01uf ceramic	1	H4
C16	.001uf ceramic	1	H5
C21,22	10pf silver mica	2	C7,C7
C28	100pf ceramic	1	G2
	TOTAL	28	

Resistors

R1,2,27	390 ohms	3	K1,K2,F4
R3,4,10,26	820	4	I1,I2,H4,H5
R6,7,17,18	1.8k	4	J3,K4,A8,B8
R8,16,5,29	1.2k	4	L5,A8,J2,G2
R9	1.6k	1	L6
R11	12k	1	H5
R12,20	33k	2	A3,A8
R13,24	39k	2	A6,A7
R14	160	1	A6
R15,22	2.7k	2	A7,J3
R19,23	20 ohm	2	C8,A7
R21,25,28	150 k	2	A6,B7
	TOTAL	28	

Voltage Regulator

VR1	78L05	1	M5

Circuit Board

1

Transistors

Q1,6,8,9,10	MPS5172	5	J3,A5,A7,A6,J8
Q2,3	NSD202	2	K1,K2
Q4,5	NSD102	2	M6,M6
Q7	MPS3638	1	C8
	TOTAL	10	

ACT-V MAIN LOGIC BOARD PARTS LIST

Diodes

Part	Description	Quantity	Location
D1	IN5242	1	K1
D2, D10, D11	IN5231	3	K2, B8, A8
D3, 4, 5, 6, 7	UA14B	5	M3, M4, M4. M4. M4
D8	IN5350	1	M8
D9	IN5339	1	M8
D12	IN4148	1	J8
	TOTAL	12	

Switches

BRS1, 2	Baud Rate Rotary	2	Rear Board
SS1	F/H Duplex Slide	1	Rear Board
US1-6	UART Option - 6 pos-Dip	1	B6
	TOTAL	4	

Sockets/Connectors

I/O, Aux., Printer Conn.	DB25SF179 Sockets	3	Rear Board
OA2, FF1, FF3	14 pin dip I.C. Sockets	3	B8, G4, A1
CR1, 2, 3, J1, J2	16 pin dip I.C. Sockets	5	B2, B7, G2, B3, E9
MPB, MPT, CG1	24 pin dip I.C. Sockets	3	C2, C1, I5
CPU, SMI, U1	40 pin dip I.C. Sockets	3	D6, D4, C4
P1, 2, 3, 4	Molex 6 pin Plugs	4	M6, M5, M4, K3
	TOTAL	21	

Crystals

XTAL1	9.828 MHz	1	J2
XTAL2	2.00 MHz	1	C6
	TOTAL	2	

```
.M 5000,53FF
5000  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00
5010  00 00 00 3F  32 24 28 24  24 24 32 28  32 22 00 00
5020  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00
5030  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00
5040  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00
5050  00 00 00 00  00 00 00 00  00 00 00 00  00 00 00 00
5060  00 00 00 00  00 00 00 21  00 00 22 00  00 00 00 00
5070  68 61 00 00  00 00 00 00  00 61 00 00  00 00 00 00
5080  1F 1F 10 18  1C 1E 08 04  04 00 00 04  1F 00 00 00
5090  00 00 00 00  2C 2E 3E 38  24 38 2C 28  2C 22 0F 1F
50A0  00 04 0A 0A  04 18 08 04  04 04 04 00  00 00 00 00
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50D0  1E 0E 1E 0E  1F 11 11 11  11 11 1F 1F  00 1F 00 00
50E0  08 00 08 00  01 00 03 66  08 00 2C 08  04 00 00 00
50F0  68 61 00 00  04 00 00 00  00 66 00 06  04 0C 00 1F
5100  11 1F 10 04  10 04 14 04  02 00 04 04  00 1F 00 00
5110  00 00 00 00  00 00 00 00  00 00 00 00  00 00 15 15
5120  00 04 0A 0A  0F 19 14 04  08 02 15 04  00 00 00 01
5130  11 0C 11 01  06 10 08 01  11 11 00 00  04 00 04 11
5140  11 0A 11 11  11 10 10 10  11 04 01 12  10 1B 11 11
5150  11 11 11 11  04 11 11 11  11 11 01 18  10 03 00 04
5160  04 00 08 00  01 00 04 00  08 04 02 08  04 00 00 00
5170  00 00 00 00  04 00 00 00  00 00 00 08  04 02 00 1F
5180  11 1F 10 18  18 08 14 1F  01 00 00 04  00 00 1F 00
5190  00 00 00 00  00 00 00 00  00 00 00 00  00 00 15 15
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5210  00 00 00 00  00 00 00 00  00 00 00 00  00 00 0F 17
5220  00 04 00 0A  0E 04 08 00  10 01 04 1F  00 1F 00 04
5230  15 04 06 06  12 01 1E 04  0E 0F 00 00  10 00 01 04
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5250  1E 11 1E 0E  04 11 11 15  04 04 04 18  04 03 0A 1F
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5270  09 09 09 08  04 09 11 15  0A 09 02 10  00 01 15 1B
5280  11 1F 02 1A  1A 0A 00 04  01 00 00 15  00 00 00 00
5290  1F 00 00 00  0C 04 0C 18  04 1C 0C 1E  0C 0C 05 11
52A0  00 04 00 1F  05 08 15 00  10 01 0E 04  04 00 00 08
52B0  19 04 08 01  1F 01 11 08  11 01 04 04  08 1F 02 04
52C0  16 1F 11 10  11 10 10 13  11 04 01 14  10 11 13 11
52D0  10 15 14 01  04 11 11 15  0A 04 08 18  02 03 11 08
52E0  00 0E 09 08  09 0F 04 09  09 04 02 0C  04 15 09 09
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5350  10 12 12 11  04 11 0A 1B  11 04 10 18  01 03 00 04
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5370  09 09 08 01  04 09 0A 15  0A 09 08 08  04 02 00 1F
5380  1F 1F 08 08  08 08 00 1F  04 00 00 04  00 00 00 00
5390  00 00 1F 00  12 04 04 18  1E 18 1C 08  0C 0E 05 1F
53A0  00 04 00 0A  04 03 0D 00  04 04 04 00  08 00 04 00
53B0  0E 0E 1F 0E  02 0E 0E 08  0E 1C 00 08  02 00 08 04
53C0  0F 11 1E 0E  1E 1F 10 0F  11 0E 0E 11  1F 11 11 0E
53D0  10 0D 11 0E  04 0E 04 11  11 04 1F 1F  00 1F 00 00
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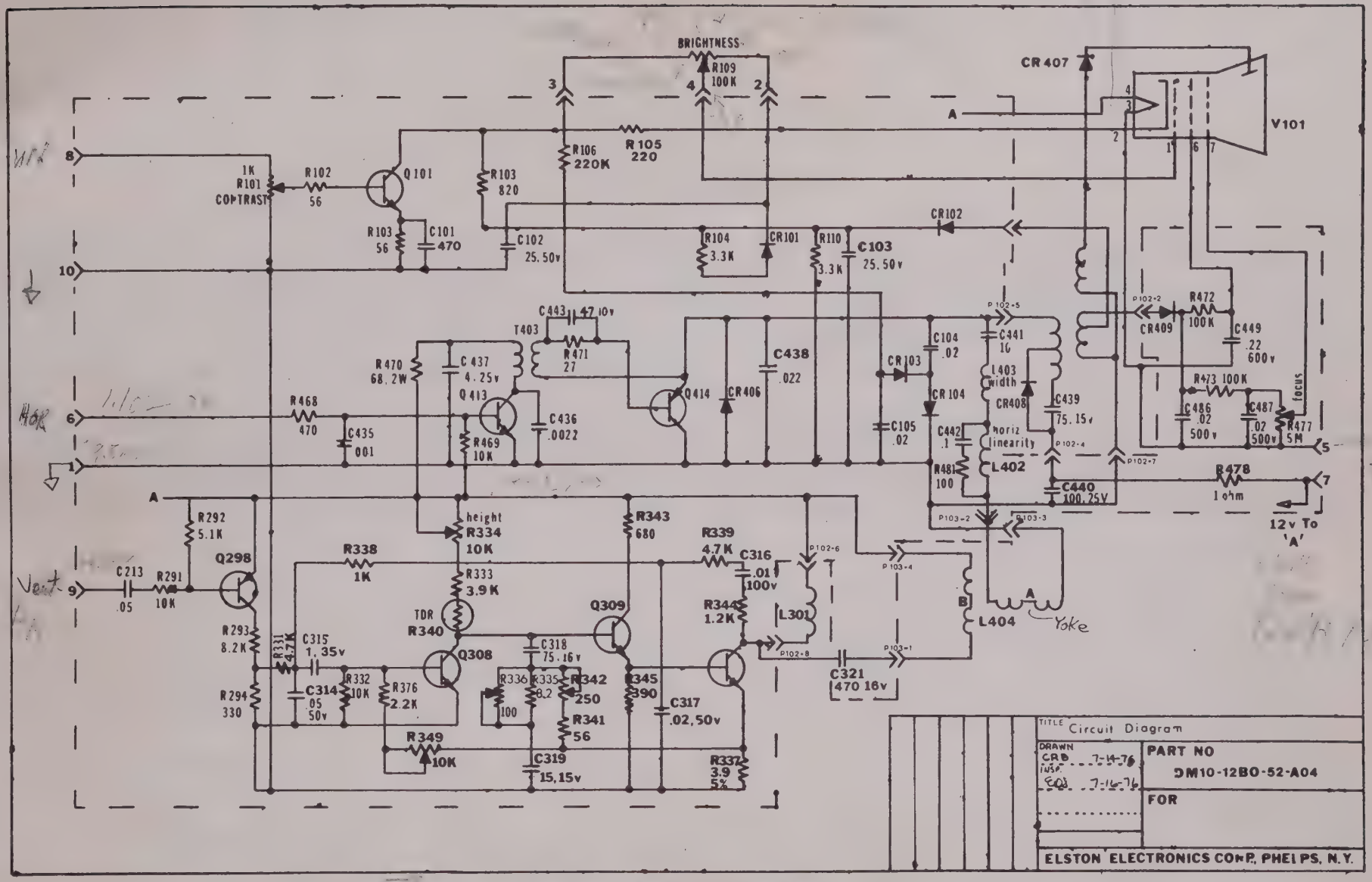
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R109 100K
CR407
V101
R106 220K
R105 220
1K R101 CONTRAST
R102 56
Q101
R103 820
R103 56
C101 470
C102 25.50v
R104 3.3K
CR101
R110 3.3K
C103 25.50v
CR102
C443 47 10v
T403
R471 27
R470 68.2W
C437 4.25v
Q413
C436 .0022
R469 10K
R468 470
C435 001
Q414
CR406
C438 .022
CR103
CR104
C104 .02
C105 .02
C441 10
L403 width
CR408
C439 75.15v
horiz linearity
L402
C442 .1
R481 100
C440 100.25V
P102-5
P102-2
CR409
R472 100K
C449 .22 600v
R473 100K
C486 .02 500v
C487 .02 500v
R477 5M
focus
R478 1 ohm
12v To 'A'
R292 5.1K
Q298
C213 .05
R291 10K
R293 8.2K
R294 330
R331 4.7K
C315 1.35v
C314 .05 50v
R332 10K
R376 2.2K
height R334 10K
R333 3.9K
TDR R340
Q308
R338 1K
R343 680
R339 4.7K
C316 .01 100v
Q309
R344 1.2K
L301
C318 75.16v
R336 100
R335 8.2
R342 250
R341 56
R345 390
C317 .02,50v
C319 15,15v
R349 10K
R337 3.9 5%
C321 470 16v
L404
Yoke
P102-6
P103-4
P103-1
P102-8
P103-2
P103-3
P102-4
P102-7
TITLE Circuit Diagram
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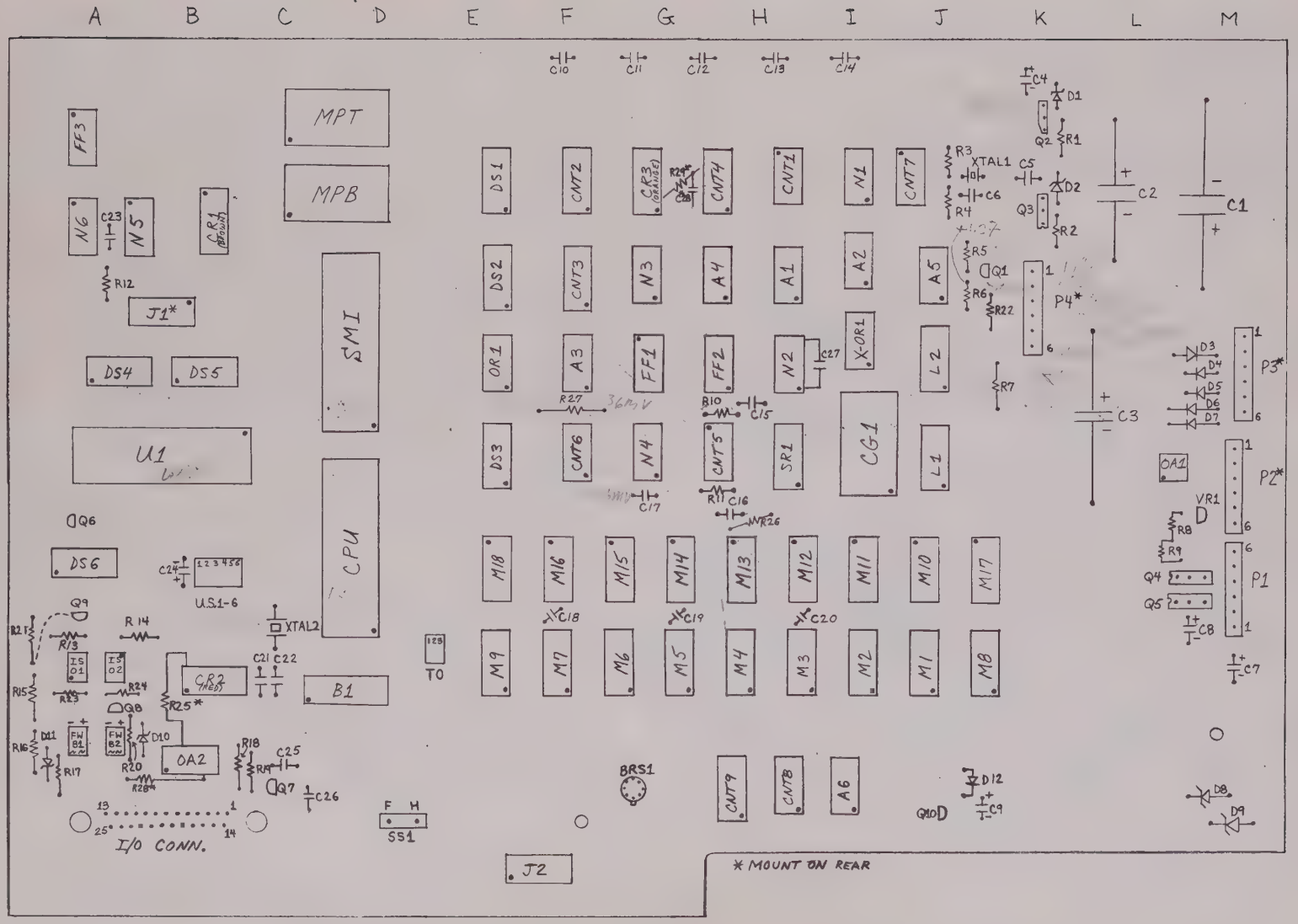
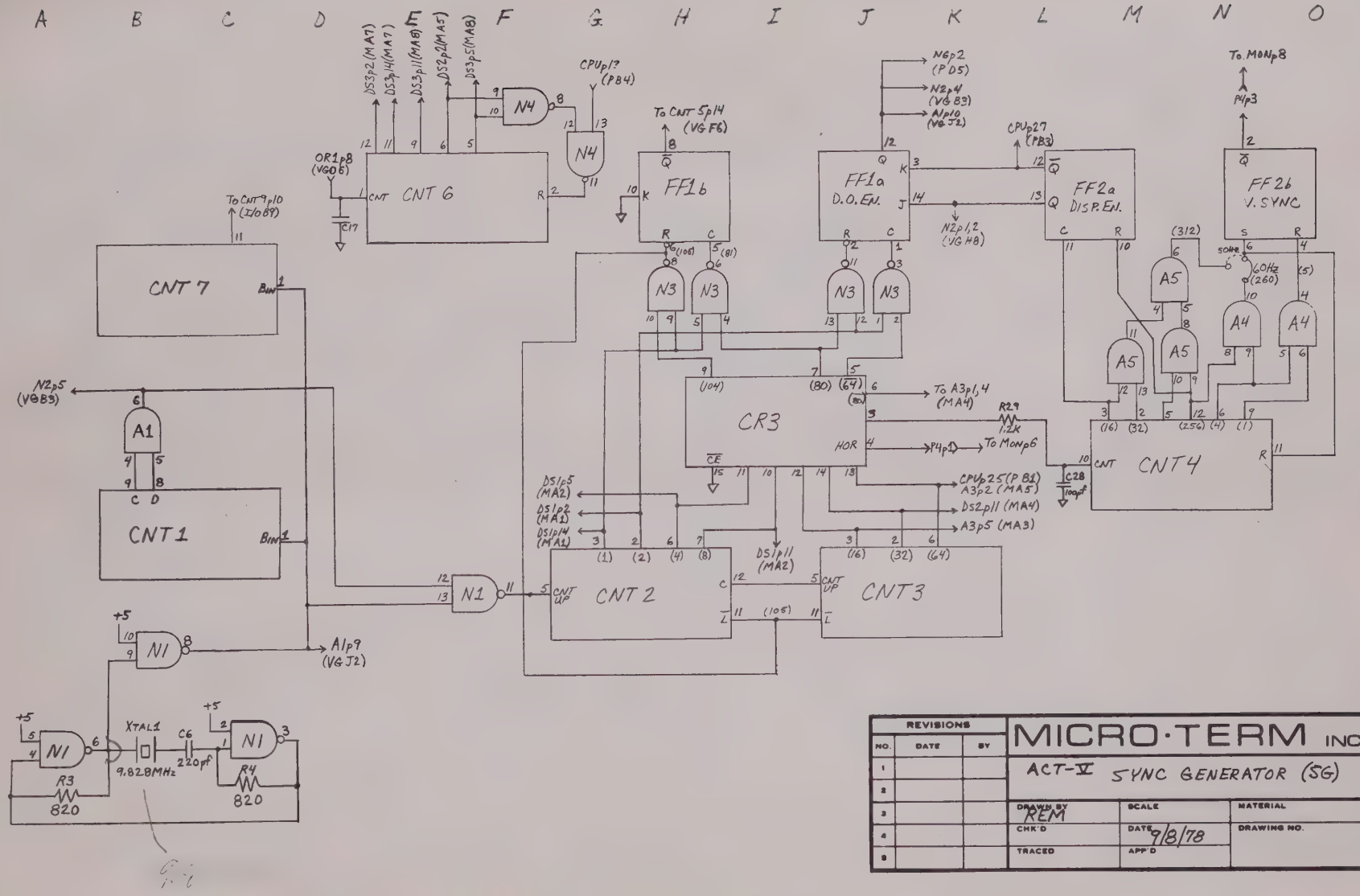
INSP. EQ 7-16-76
PART NO DM10-12BO-52-A04
FOR
ELSTON ELECTRONICS CORP. PHELPS, N.Y.



PARTS LOCATION (VIEWED FROM COMPONENT SIDE)



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NO.	DATE	BY	ACT-V SYNC GENERATOR (SG)
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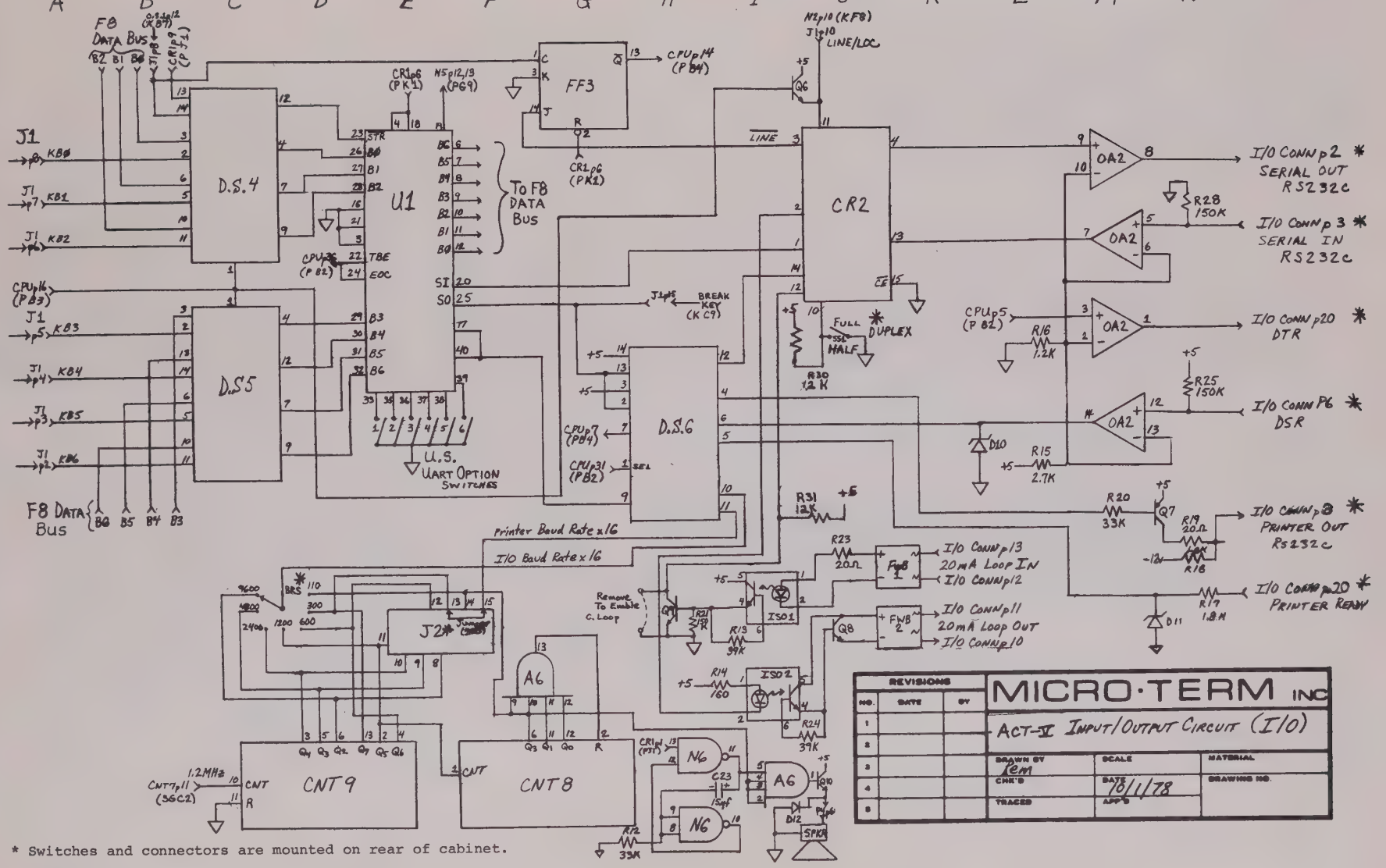
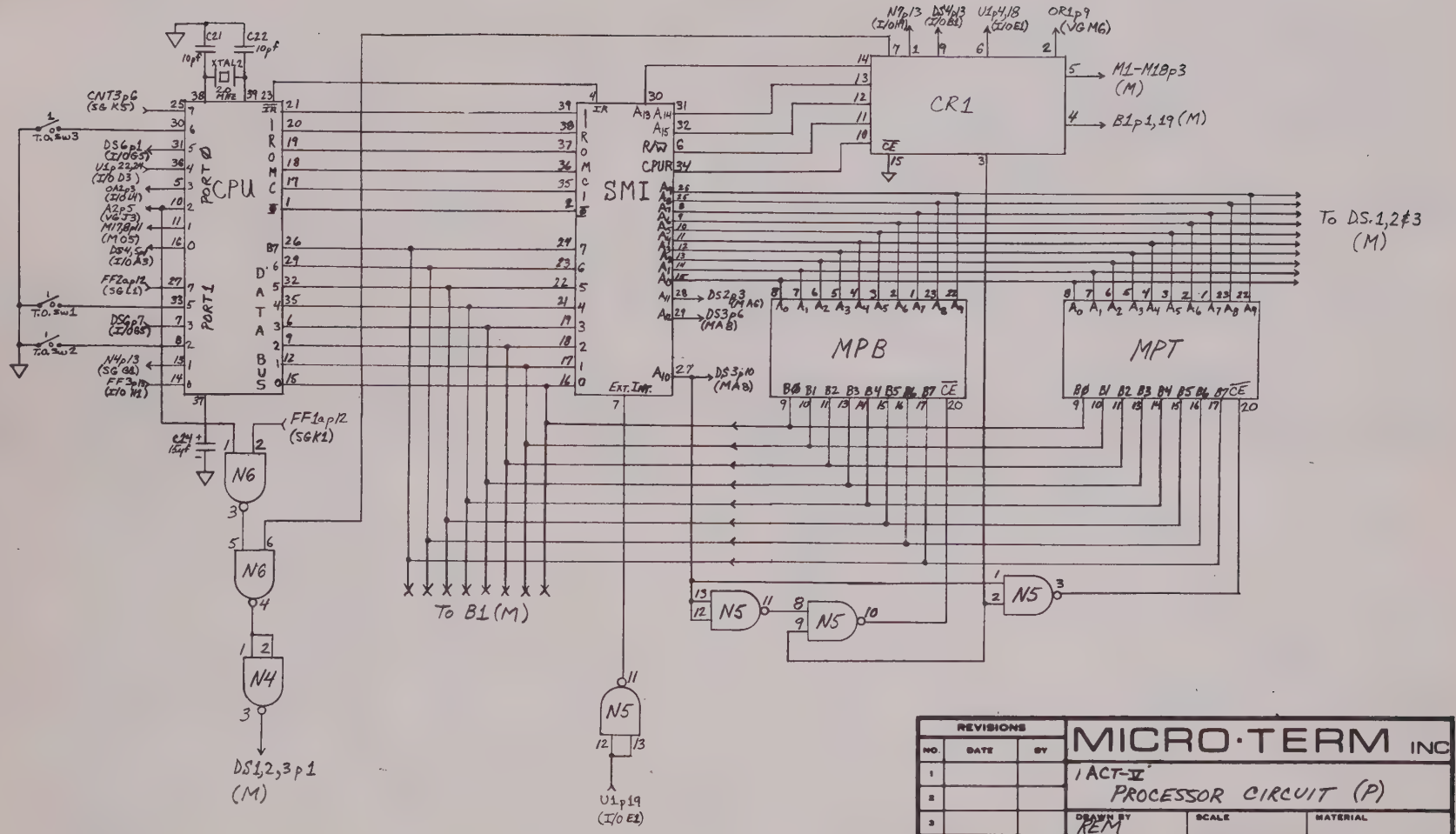
2			
3			DRAWN BY REM / SCALE / MATERIAL
4			CHK'D / DATE 9/8/78 / DRAWING NO.
5			TRACED / APP'D



REVISIONS			MICRO·TERM INC
NO.	DATE	BY	ACT-V Input/Output Circuit (I/O)
1			
2			
3			
4			
5			

DRAWN BY	SCALE	MATERIAL
Tem		
CHK'D	DATE 10/11/78	DRAWING NO.
TRACED	APP'D	

* Switches and connectors are mounted on rear of cabinet.



REVISIONS		
NO.	DATE	BY
1		
2		
3		
4		
5		

MICRO·TERM INC

ACT-II
PROCESSOR CIRCUIT (P)

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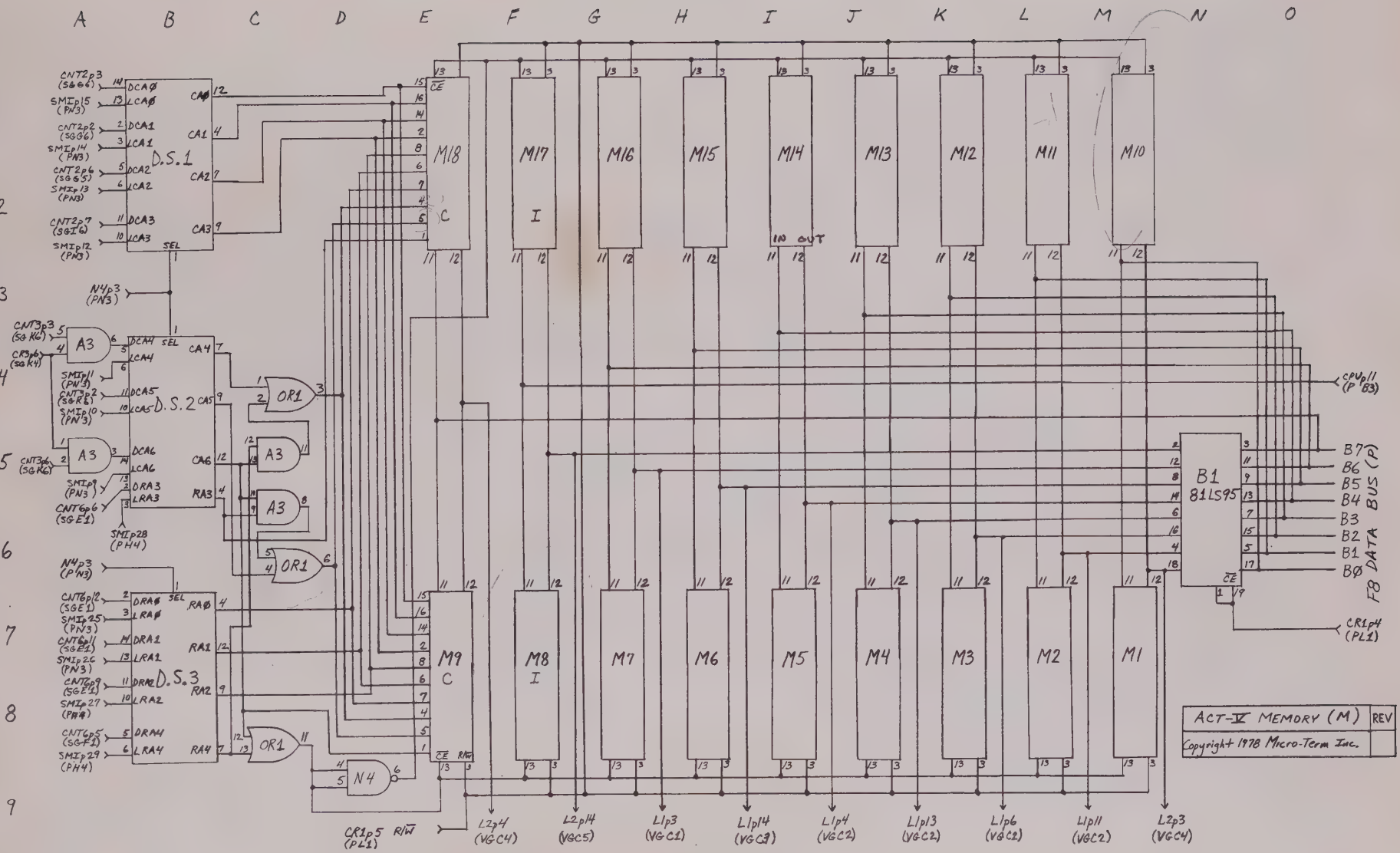
CHK'D	DATE 9/8/78	DRAWING NO.
TRACED	APP'D	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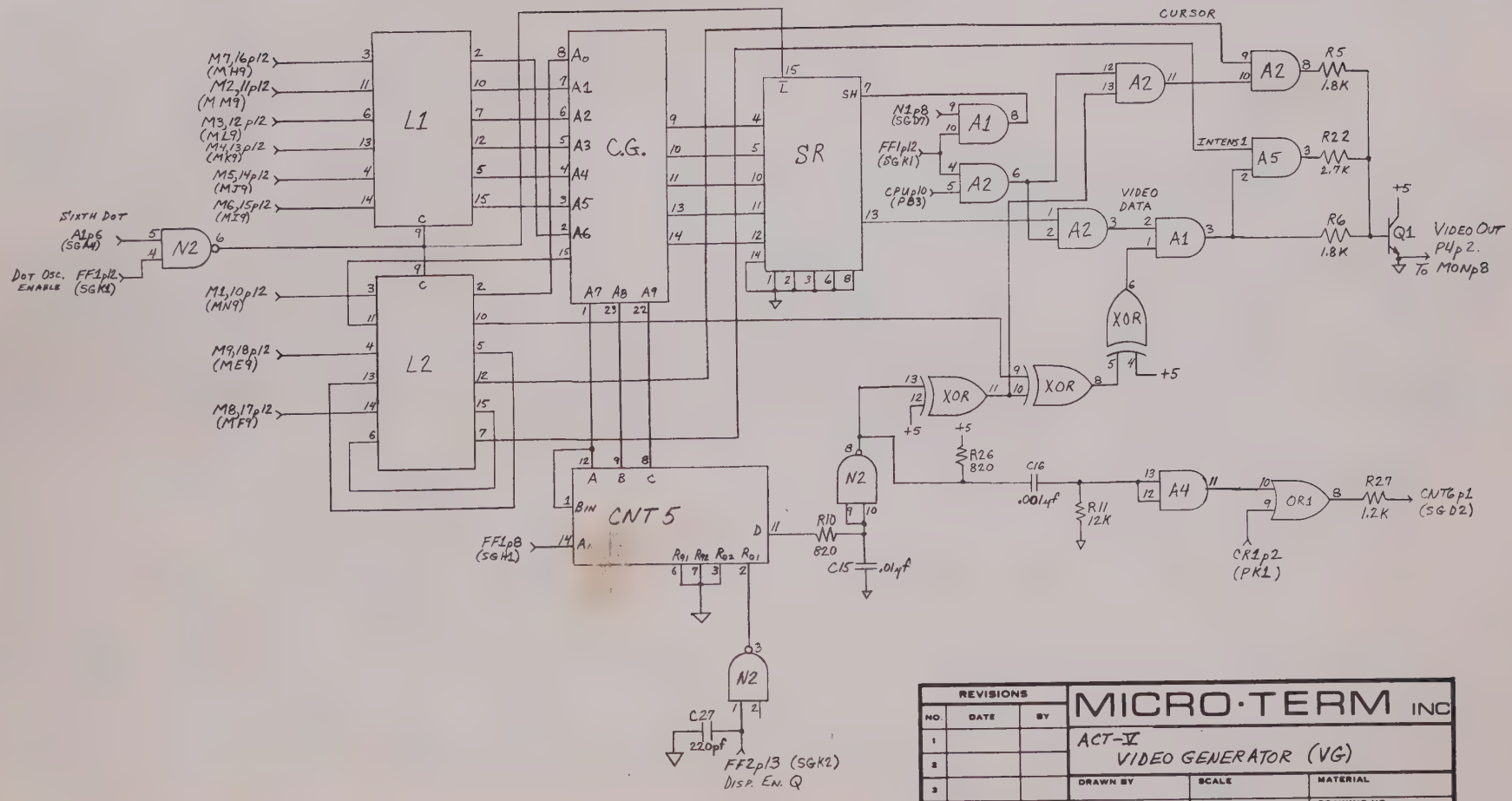
D.S.1
D.S.2
D.S.3
M18 C
M17 I
M16
M15
M14
M13
M12
M11
M10
M9 C
M8 I
M7
M6
M5
M4
M3
M2
M1
B1 81LS95
A3
OR1
N4
CNT2p3 (SG66)
SMIp15 (PN3)
CNT2p2 (SG66)
SMIp14 (PN3)
CNT2p6 (SG65)
SMIp13 (PN3)
CNT2p7 (SGIH)
SMIp12 (PN3)
N4p3 (PN3)
CNT3p3 (SGKG)
CR3p6 (SGK4)
SMIp11 (PN3)
CNT3p2 (SGKB)
SMIp10 (PN3)
CNT3p6 (SGKG)
SMIp9 (PN3)
CNT6p6 (SGE1)
SMIp28 (PH4)
CNT6p12 (SGE1)
SMIp25 (PN3)
CNT6p11 (SGE1)
SMIp26 (PN3)
CNT6p9 (SGE1)
SMIp27 (PH4)
CNT6p5 (SGF1)
SMIp29 (PH4)
CR1p5 R/W (PL1)
L2p4 (VGC4)
L2p14 (VGC5)
L1p3 (VGC1)
L1p14 (VGC3)
L1p4 (VGC2)
L1p13 (VGC2)
L1p6 (VGC2)
L1p11 (VGC2)
L2p3 (VGC4)
CPUp11 (P 83)
CR1p4 (PL1)
B7
B6
B5
B4
B3
B2
B1
BØ
F8 DATA BUS (P)
IN OUT
ACT-V MEMORY (M)
REV
Copyright 1978 Micro-Term Inc.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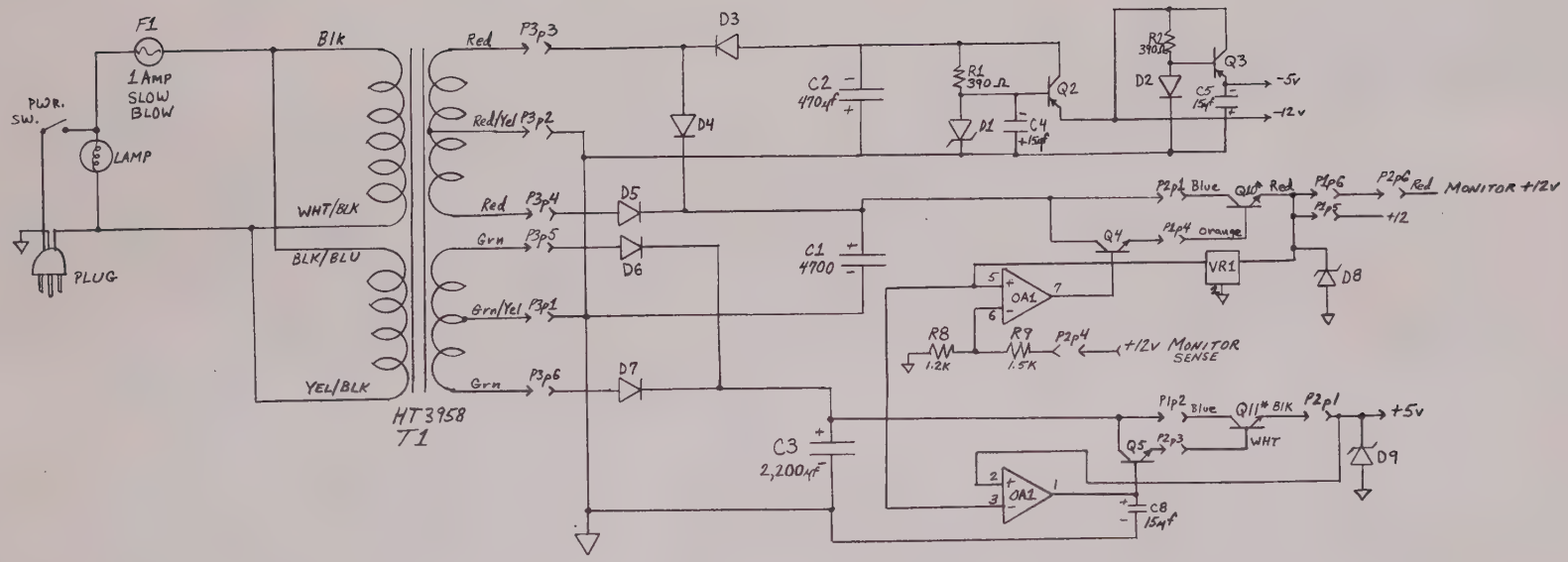
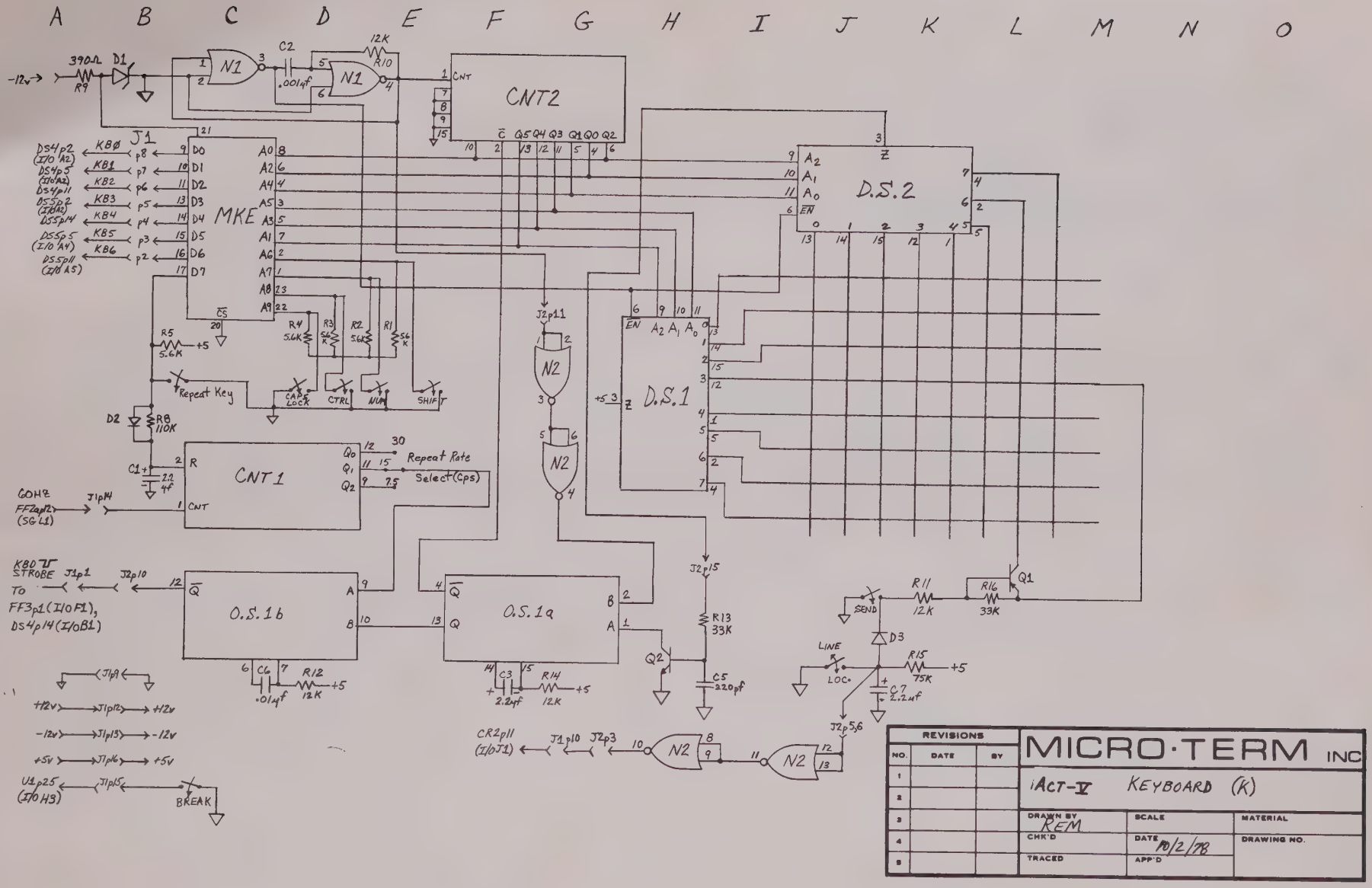
CURSOR
M7,16p12 (MH9)
M2,11p12 (MM9)
M3,12p12 (ML9)
M4,13p12 (MK9)
M5,14p12 (MJ9)
M6,15p12 (MI9)
L1
C.G.
SR
SH
N1p8 (SGD7)
FF1p12 (SGK1)
CPUp10 (PB3)
A1
A2
A5
INTENS1
R5 1.8K
R22 2.7K
R6 1.8K
+5
Q1
VIDEO OUT P4p2. To MONp8
VIDEO DATA
SIXTH DOT
A1p6 (SGA4)
N2
DOT OSC. ENABLE
FF1p12 (SGK1)
M1,10p12 (MN9)
M9,18p12 (ME9)
M8,17p12 (MF9)
L2
XOR
R26 820
C16 .001μf
R11 12K
A4
OR1
R27 1.2K
CNTGp1 (SGD2)
CR1p2 (PK1)
CNT5
FF1p8 (SGH1)
R10 820
C15 .01μf
C27 220pf
FF2p13 (SGK2) DISP. EN. Q
REVISIONS
NO. DATE BY
MICRO·TERM INC
ACT-V VIDEO GENERATOR (VG)
DRAWN BY
CHK'D
TRACED
SCALE
DATE 9/8/78
APP'D
MATERIAL
DRAWING NO.



* Q10 and Q11 are mounted on cabinet

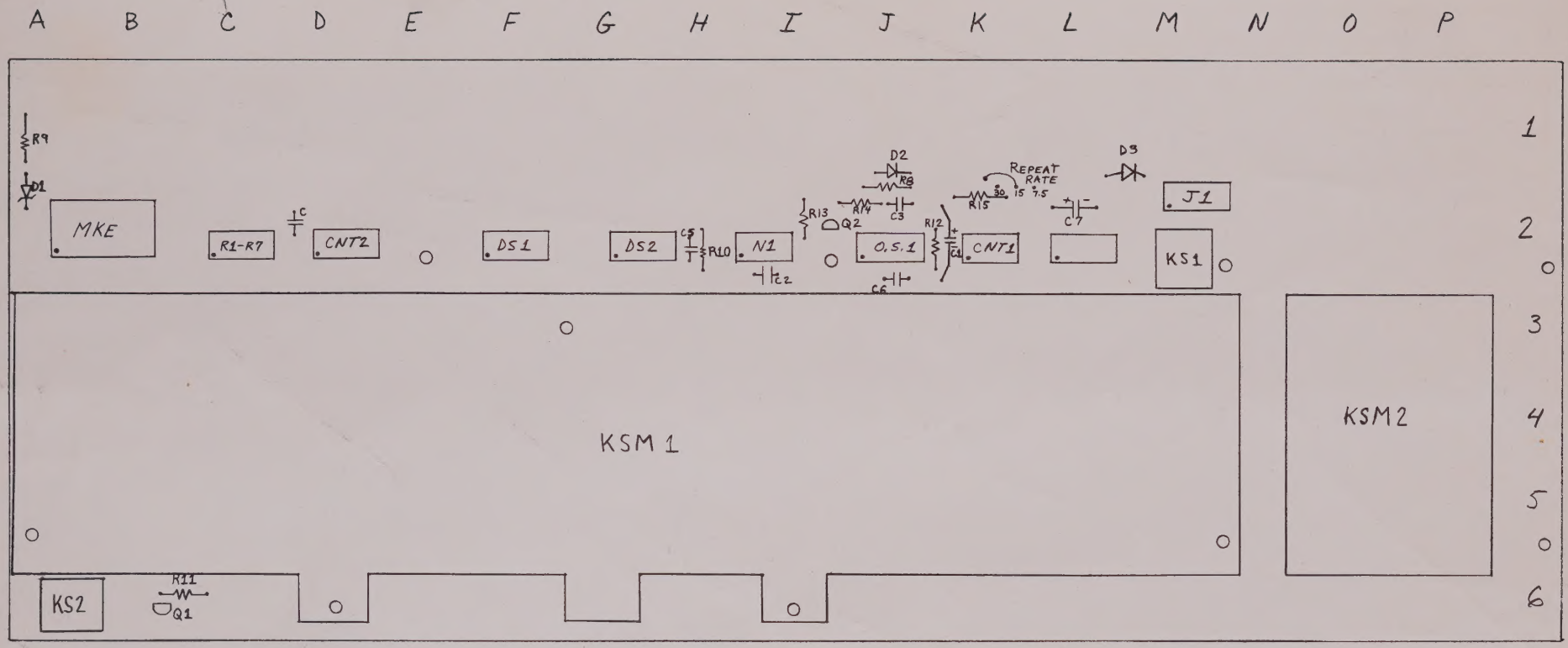
REVISIONS			MICRO·TERM INC
NO.	DATE	BY	ACT-V POWER SUPPLY (PS)
1			
2			
3			DRAWN BY Rem / SCALE / MATERIAL
4			CHK'D / DATE 10/13/78 / DRAWING NO.
5			TRACED / APP'D



REVISIONS			MICRO·TERM INC	
NO.	DATE	BY	iACT-V KEYBOARD (K)	
1				
2				
3			DRAWN BY REM	SCALE
4			CHK'D	DATE 10/2/78
5			TRACED	APP'D

MATERIAL

DRAWING NO.



ACT-II KBD PARTS LAYOUT

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